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Applicant: (Name and address)
Danfoss A/S
Nordborgvej 81
6430 Nordborg
Denmark

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Patentansøgning

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Patent- og Varemærkestyrelsen
Erhvervsministeriet

Helgeshøj Allé 81
2630 Taastrup

Tlf. 43 50 80 00
Fax 43 50 80 01
Postgiro 8 889 923
E-post pvs@dkpto.dk
www.dkpto.dk

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Danfoss A/S
DK - 6430 Nordborg

Telefon: 74 88 22 22 Telefax:

5. Fuldmægtig (navn og adresse):

Danfoss A/S
Patentafdelingen
DK - 6430 Nordborg
Telefon: 74 88 34 97 Telefax: 74 88 20 03

6. Opfinder (fornavn, efternavn, adresse):

Aksel Baagø Jepsen
Solsikkevej 6
DK - 6440 Augustenborg

6a. Opfinder (fornavn, efternavn, adresse): ☐ Flere opfindere på bagsiden

Nils-Ole Harvest
Skovtoften 11
Havnbjerg
DK- 6430 Nordborg

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Frank Petersen
Frank Petersen

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Modtaget
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PVS

Danfoss A/S

DK-6430 Nordborg
Danmark
Reg.No.: 31744

Telephone: +45 74 88 22 22
Telefax: +45 74 49 09 49
Telex: 50 599 danfss dk

E-mail: danfoss@danfoss.com
Homepage: www.danfoss.com

Patent og Varemærkestyrelsen
Helgeshøj Alle 81
2630 Taastrup

Deres ref./Your ref./Ihr Zeichen	Vor ref./Our ref./Unser Zeichen	Dato/Date/Datum	Gennemvalgsnr./Direct dialling/Durchwahl
	02 01 571 030	23.juni 2002	Email: fp@danfoss.com Fax: +45 7488 2003 Phone: +45 7488 34 97

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Vedlagt fremsendes engelsksproget ny patentansøgning bestående af

- ansøgningsformular	1 side
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Danfoss A/S

Frank Petersen

1

Power converter

The invention concerns a power converter for use in green power applications and particularly a module concept. "Green power" is the term used for energy sources like wind, sun or fuel cells, and the inventive power converter can be used for these different sources of electrical energy.

The power generated by green power units is converted into a voltage and a frequency suited to the commercial mains. Conversion is typically done by using a switch mode DC/DC converter followed by a conversion into AC. DE 199 19 766 A1 describes the use of paralleled DC/DC converters that are electrically connected to the same DC/AC inverter. In this way, all DC/DC converters feed energy to a common DC bus, and advantageously only one DC/AC inverter is used. Thus, a green power inverter unit is made which consists of several DC/DC modules connected to a DC/AC inverter.

It would be of interest to enable a control of each of the modules used in the system. The object of the invention is to provide a sufficient, yet easy, form of controlling power modules used inside a power converter.

This is done with a power converter according to the independent claim.

Advantageously, a system with distributed intelligence is achieved. As each module has its own controller, galvanically separated from the other controller, and communicating via a bus, each module controls itself according to commands received from other modules. Thus, a high degree of load management and load distribution is possible. But also flexibility is achieved. Exchanging a photovoltaic DC/DC module with a fuel cell module is possible, because the controller on the module has all control strategies at hand. The same DC/AC inverter can be used

II

Figure 1.22A shows a photovoltaic cell P feeding direct current to an H-bridge DC/DC converter.

The control of the total system is divided into two control circuits 1 and 2 galvanically isolated from each other. In this embodiment, a micro controller regulates the converter, and a Digital Signal Processor regulates the inverter. The DC/DC converter and controller are placed on a first module A and inverter and controller are placed on a second module B. In this way, a modularized system is achieved, which makes customisation easy. Thus, in the case where the energy cell is not a photovoltaic cell but a fuell cell, module A is replaced by modul A' or A" comprising a control and a DC/DC converter suited for a fuel cell, which supplies a lower voltage than the photovoltaic cell. Or, alternatively, the inverter module B can be replaced. Also, the Man-Machine Interface M is an intelligent module with communication capability. The concept of modularization may be extended further as shown in Figure 1.22B and 1.22 C. In Fig.1.22B Cu indicates custom specific green power inverters, which consists of modules. Such modules – typically printed circuit boards – are indicated by the term PCB. Instead of having a large modul A, the DC/DC converter may consist of several smaller submodules e.g. controller 3 and power module 4. Controller 3 communicates with the power board 5 via serial bus 6.

Fig.1.22 C shows how a DC-module A is connected to a DC-bus, which is common to several other DC converters. They are all feeding energy into the DC-bus, and DC/AC inverter B taps the DC bus and converts the energy into a grid voltage and frequency. A filter as described in this application may be used. Such filter is also a module, as shown with F in Fig.1.22 A. The modules are connected to each other via an interface I shown on Figure 1.22A. Such interface is preferredly an easy insertion interface. The modules communicated via a serial bus. The CAN bus is preferred.

III

In summary, by dividing the green power inverter into a DC/DC converter and an inverter, adding control intelligence to each module, the possibility of a modular system is opened. The converter and the inverter can be designed separately, and fx changing the DC/DC converter topology can be done without changing the inverter topology. Thus, the green power unit is flexible on a system level as well as on a converter technology level.

Turning to Fig.1. 22A, the DC-DC converter control is connected to minus M1 of the converter, i.e. to minus of the solar cell P. This simplifies the gate drives and no extra power supplies and optoisolators are needed. Current measurement may be made with a shunt in the minus, but a resistor RM1 inserted serially in the power leg is preferred. Further, input reference signals from the outside world would be on low potential.

Also, the inverter control is connected to minus M2 of the DC/AC inverter. This simplifies gatedrives and supply for these, since bootstrap supply based gatedrive IC's could be used. Since the inverter voltage loop always operates at fixed voltage reference (375 V) an external reference is not needed for this subcircuit.

Startup or shut-down signals between the two circuits, i.e. the first and the second controller, may easily be transferred with inexpensive optocouplers. This can be done by means of the serial bus.

The modular concept enables the distribution of intelligence. Instead of having one master controlling all modules, each module A, A', B or M has its own controller and communication interface. This also accounts for the case, where e.g. the DC/DC converter consists of submodules 3,4 and 5.

IV

Claims

1. Power converter comprising a DC/DC converter and a DC/AC inverter where energy from the DC/DC converter is transferred to the DC/AC inverter and where the DC/DC converter forms a first module and the DC/AC inverter a second module characterized in that the DC/DC converter (A) comprises power switches which are controlled by a first controller (1), that the DC/AC inverter (B) comprises power switches controlled by a second controller (2), where the first and second controller are galvanically isolated from each other, and where the first and second controller each incorporates a serial communication interface and communicates with each other via a galvanically separated serial bus.

2. Power converter according to claim 1 characterized in that the DC/DC converter and the DC/AC converter respectively consists of several submodules, one submodule being a control module, another submodule being a power switch module.

3. Power converter according to one of the preceeding claims characterized in that the first controller is connected to minus of the DC/DC converter, and that the second controller is connected to minus of the DC/AC inverter.

4. Power converter according to one of the preceeding claims characterized in that a man-machine interface module is connected to the serial communication bus.

5. Power converter according to one of the preceeding claims characterized in that the DC/DC converter comprises an H-bridge of power switches, and that the DC/AC inverter also comprises an H-bridge of power switches.

V

6. Power converter according to claim 5 characterized in that at least one current sensor, preferably a shunt, is inserted in a leg of the H-bridge in the converter and the inverter respectively, and that the current signals are led to the first and second controller respectively.

7. Power converter according to one of the preceeding claims characterized in that the converter is current controlled and that the inverter is voltage controlled.

8. Power converter according to claim 1 characterized in that other DC/DC converters or other DC/AC inverters communicate with the controllers (1,2) via the serial bus.

Abstract

Power converter

The invention concerns a power converter for use in green power applications, and particularly a module concept. ."Green power" is the term used for energy sources like wind, sun or fuel cells, and the inventive power converter can be used for these different sources of electrical energy. It is of interest to enable a control of each of the modules used in a green power inverter system. This object is reached in that a DC/DC converter (A) comprises power switches which are controlled by a first controller (1), that the DC/AC inverter (B) comprises power switches controlled by a second controller (2), and that the first and second controller are galvanically isolated from each other. Further, the first and second controller each incorporates a serial communication interface and communicates with each other via a galvanically separated serial bus.

Abstract— This paper presents a new grid connected inverter for fuel cells. It consists of a two stage power conversion topology. Since the fuel cell operates with a low voltage in a wide voltage range (25V-45V) this voltage must be transformed to around 350-400V in order to invert this dc power into ac power to the grid. The proposed converter consists of an isolated dc-dc converter cascaded with a single phase H-bridge inverter. The dc-dc converter is a current-fed push-pull converter. A new dedicated voltage mode startup procedure has been developed in order to limit the inrush current during startup. The inverter is controlled as a power factor controller with resistor emulation.

Experimental results of converter efficiency, grid performance and fuel cell response are shown for a 1 kW prototype. The proposed converter exhibits a high efficiency in a wide power range (higher than 92%) and the inverter operates with a near unity power factor and a low current THD.

I. Introduction

GREEN power(renewable power) becomes increasingly more important due to global pollution problems. There exist many different types of green power technologies such as wind turbines, photovoltaic cells and fuel cells. Wind turbines and photovoltaic cells are well known and matured technologies but both have an obvious disadvantage: these technologies delivers only power when the wind blows/the sun is shining. Thus, these technologies cannot be used as primary power supply in the grid.

Fuel cells can produce power (electrical and thermal) when supplied with fuel and fuel cells(in some technologies) can have bidirectional power flow. In this case the fuel cell can therefore operate as an energy storage. A fuel cell system can also be used as an uninterruptable power supply for a house, a factory or a village. Fig. 1a shows a typical electric-characteristic of a fuel cell.

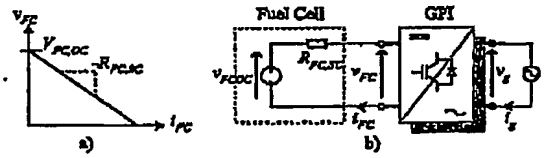


Fig. 1. Green power inverter for fuel cells. a) Fuel cell characteristic and b) Fuel cell and inverter.

Many converter topologies are investigated in the literature for photovoltaic cells and for fuel cells [2]-[11]. The different converter topologies are compared with regards to the converter efficiency and cost.

This paper deals with a grid connected fuel cell converter. In order to utilize the fuel as good as possible the fuel cell converter/Green Power Inverter (GPI) must have a high and broad efficiency characteristic. It is important to notice that the input voltage to the GPI (v_{FC}) is variable and that v_{FC} decreases with increasing power (cf. fig. 1a). The power range of the fuel cell investigated in this paper is 1 kW peak power at 25 V and the the no load voltage is 45 V.

In section II the reason for choosing the proposed converter is given. Next the functionality and design aspects of the dc-dc converter are described. In section IV the hardware of the grid connected inverter is given and section V describes the control of the whole green power inverter. Finally experimental results are shown.

II. Topologies for Green Power Inverters

The special application must be considered in order to select a proper converter topology and the overall performance requirements to the GPI are

- to control the fuel cell voltage according to a given reference,
- to deliver a grid current with a high power factor and a low current THD,
- to have a high efficiency in the whole operating range,
- the high frequency ripple of the fuel cell current should be small,
- the cost should be minimized.

In addition, the GPI must provide galvanic isolation between the fuel cell terminals and the utility grid. Since the fuel cell operates in the voltage range 25-45 V_{dc} and the grid voltage is 230 V_{rms} the GPI must perform two tasks: The power must be inverted and the voltage must be amplified. As shown in Fig. 2 these tasks could either be done by connecting an inverter to the fuel cell followed by a 50 Hz transformer(AC-AC voltage gain) or by connecting a switch mode DC-DC converter to the fuel cell (DC-DC voltage gain) followed by a grid connected inverter.

A DC-DC voltage gain (switch mode DC-DC converter) is preferred in order to limit physical size and the cost of the system. Hence, a system with a switch-mode DC-DC converter followed by a grid connected inverter as in Fig. 2b is selected. In addition, using a grid connected inverter makes the GPI system more modular as the DC-DC converter can be replaced according to the application and a standard inverter system can

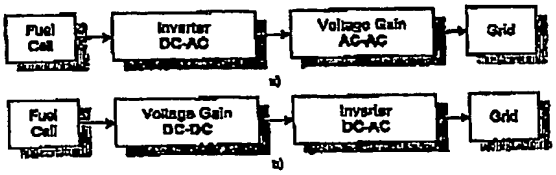


Fig. 2. Schematic description of the GPI. a) Voltage gain in AC-AC stage and b) voltage gain in DC-DC stage.

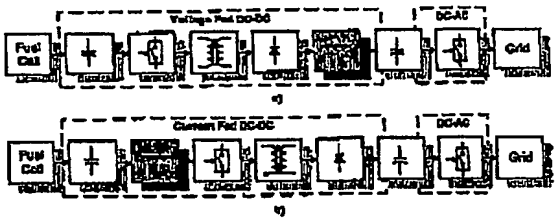


Fig. 3. Power converter topologies for GPI. a) Voltage fed converter and b) current fed converter.

be employed.Basically, the DC-DC converter can be a current fed or a voltage fed converter (cf. Fig. 3). A current fed DC-DC requires less input filtering in order to minimize the high frequency current ripple drawn by the GPI because the inductor is placed at the input.

Thus, a current fed DC-DC converter is selected. The two most attractive DC-DC converter topologies are the push-pull converter and the full-bridge converter. Both topologies exhibit a high efficiency capability. They are well known technologies and have a good utilization of the magnetics (bidirectional magnetization of the transformer). The push-pull topology is selected in order to decrease the conduction losses in the switches due to the low fuel cell voltage. The three most attractive single phase inverter topologies are the full-bridge/H-bridge inverter, the half-bridge inverter and the push-pull inverter. A standard H-bridge inverter is selected due the good utilization of the materials and a high efficiency capability. The GPI topology depicted in Fig. 4 is proposed for a grid connected fuel cell converter in the power range of 1 kW.

A snubber circuit is used to protect the MOSFETs in the push-pull converter due to the leakage inductance of the transformer.

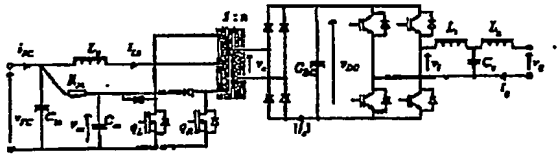


Fig. 4. Proposed Green Power Inverter topology with a push-pull stage.

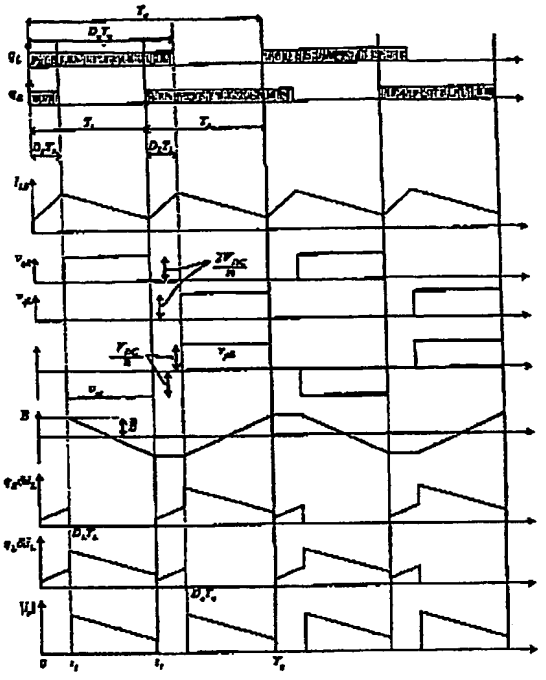


Fig. 5. Waveforms for the current-fed push pull converter in continuous conduction mode.

III. Current Fed Push-Pull Converter

The current-fed Push-Pull converter topology is described in [7]-[10]. As shown in Fig. 4, the current-fed push-pull dc-dc converter is basically an isolated boost converter and the steady state voltage transfer function for continuous conduction mode is:

$$V_{dc} = \frac{n}{1 - D_L} V_{FC} \qquad (1)$$

where D_L is the duty-cycle seen from the inductor as it can be observed in Fig. 5.

Inspecting Fig. 5 yields the following coherence between inductor duty-cycle D_L and switch duty-cycle D_q:

$$D_q = \frac{D_L + 1}{2} \qquad (2)$$

It appears that the frequency seen from the inductor is twice the switching frequency (ie. $f_L = 2f_q$). Fig. 5 shows waveforms in steady state for current mode operation ($D_q \geq 0.5$).

The used pwm modulator (SG3525 cf. [12]) is not ideal and an offset in the inductor(overlapping) duty-cycle is present in the system(cf. Fig. 6). The input to the pwm modulator is the control voltage that gives a duty-cycle

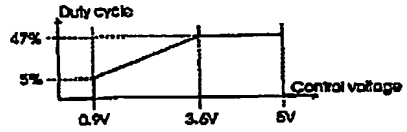


Fig. 6. Transfer characteristic of the used IC SG3525 analog PWM generator. Duty cycle is inductor duty cycle.

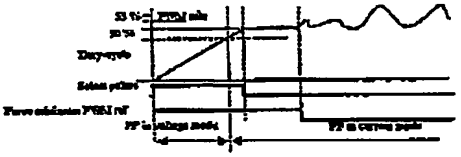


Fig. 7. Evolution of the Push Pull control signals during startup. PP: push-pull.

according to Fig. 6. Thus, the minimum inductor duty-cycle is 5%. This gives rise to a high startup current which may trigger the over-current protection and the system can therefore be difficult to start.

Due to the duty-cycle offset a new smooth startup procedure has been developed (see Fig. 7). Initially the converter is started in voltage mode ($D_q \leq 0.5$) and the switch duty-cycle is ramped up from zero to one half. When the switch duty-cycle reaches 0.5 the control IC is allowed to operate. When the push-pull converter operates in voltage mode the micro processor (see section V) provides gate signals to the MOSFETs and when the push-pull converter operates in current mode the SG3525 pwm modulator provides the gate signals. The micro-processor dictates the operating mode of the push-pull converter: The 'select pulses' is used to select the source of the gate signals. In addition, the 'force minimum PWM ref' is used to force the pmw reference of the analog control to be minimal during the transition from voltage mode to current mode. When the push-pull converter has entered current mode operation the analog control IC is released.

Fig. 8 shows the test of the implemented startup procedure. Still an inrush current is present but it is reduced and far below the over current protection limit so a smooth startup is achieved.

Fig. 9 shows experimental steady state converter waveforms at 600 W and at 1000 W. There is a good coherence between the sketched waveforms in Fig. 5 and the experimental waveforms in Fig. 9. In addition, the switch current reveals that there is a good coupling between the two primary transformer windings.

The transformer is the key component when designing the current fed push-pull DC-DC converter due to the demand for a high efficiency. A high efficiency demands for a good magnetic coupling between the two primary windings in order to decrease the power dissipated in a snubber circuit. The primary windings are

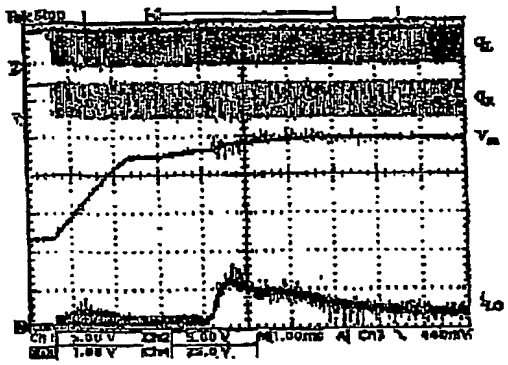


Fig. 8. Measured transition from voltage mode control to current mode control. The two top traces are gate signals, the middle trace is the voltage (v_{sw}) of the snubber circuit (see Fig. 4) and the bottom trace is the inductor current (i_{LO}). (ch3: 10A/div).

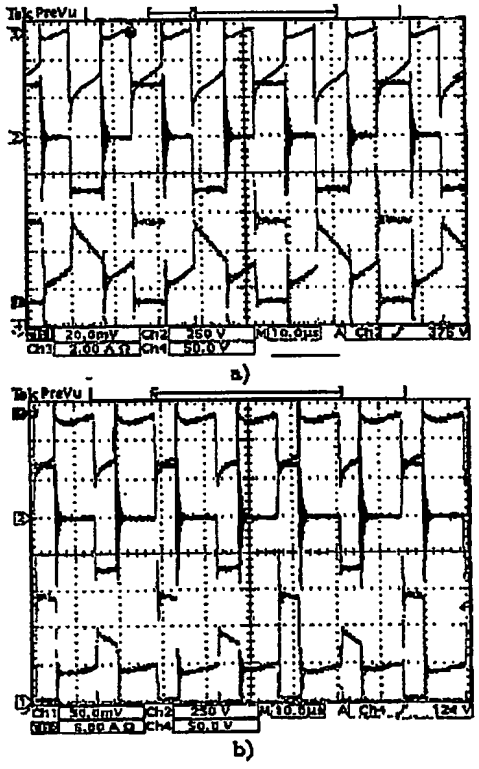


Fig. 9. Measured steady state waveforms of the current fed push pull converter. Signals from top to bottom: (ch3) negative of the rectified current ($-|i_s|$), (ch2) secondary voltage, (ch4) primary switch voltage and (ch1) switch current. a) 600 W(ch1: 10A/div) and b) 1000 W(ch1: 25A/div).

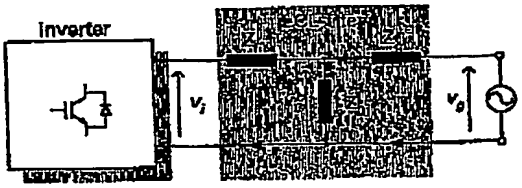


Fig. 10. Line-filter configuration at the output stage of the green power inverter.

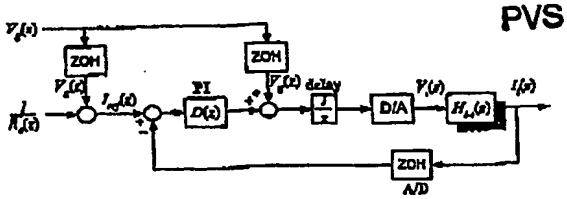


Fig. 11. Control block for the current loop.

the most important part in the transformer design due to the high coupling requirement and the high current through these windings. Different types of magnetic designs were tested and a transformer with copper foil for the primary windings gave the best coupling between the two primary windings. This solution also gave the best efficiency since the foil windings provided a good utilization of the winding area and thereby allowing a lower current density in the transformer.

IV. Inverter with filter

As shown in Fig. 4 a conventional single phase H-bridge inverter is used as DC/AC converter and a LCL-filter is selected at the output in order to achieve a high filtering of the inverter current. The inverter-filter configuration is shown in Fig. 10.

The LCL-filter has the following components in the s-domain:

$$Z_i = R_i + L_i s \quad (3)$$

$$Z_g = R_g + L_g s \quad (4)$$

$$Z_0 = \frac{1}{Cs} \quad (5)$$

and the parameters are given in Table I.

TABLE I

Line filter parameters. R_i and R_g are DC-values.

L_i [mH]	R_i [mΩ]	L_g [μH]	R_g [mΩ]	C [μF]
4.0	400	850	180	2.2

The aim of the inverter control is to load the DC-link capacitor in order to maintain the average of the dc-link voltage at the desired value $V_{dc,ref}$. The current impressed into the utility grid must comply with IEC-61000-3-2 [1]. In addition, the inverter must be fast enough to protect the dc-link and the semiconductors from over-voltages due to power processing from the power source. In order to fulfill the low harmonic regulation IEC 61000-3-2, the inverter is controlled to emulate a resistor R_e [2]. Hence, the grid current waveform must be a scalar of the voltage waveform: $R_e = v_g/i_g$ (cf. Fig. 11). The control is done digitally.

The emulated resistance R_e determines the amplitude of the grid current and the current reference I_{ref} is

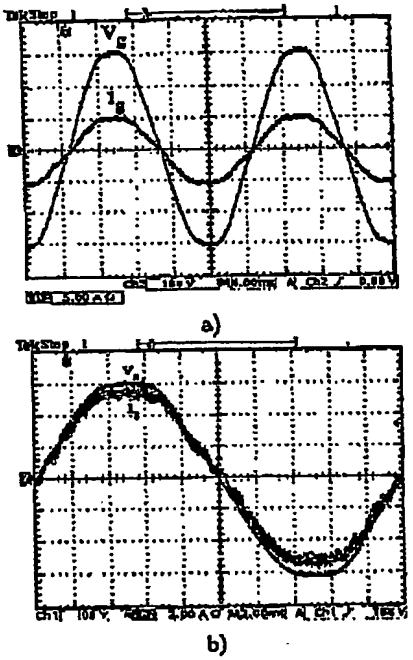


Fig. 12. Grid current at a) 800W (5 A/div) and b) 1000W (2 A/div).

formed by multiplying the measured grid voltage V_g and $1/R_e$. A conventional PI-controller is used to shape the grid current. As shown in Fig. 11 a feedforward of the measured grid voltage is used to reduce the dynamic requirements to the PI-controller. The delay corresponds to the delay associated with digital control. The transfer function $H_{i-i}(s) \triangleq I_i(s)/V_i(s)$ is the transfer function from the inverter voltage $V_i(s)$ to the inner inductor current $I_i(s)$ of the LCL filter (cf. Fig. 10).

Fig. 12 shows grid current and grid voltage at 800 W and at 1 kW. The switching frequency and the sampling frequency are both 10 kHz.

V. System Control

Fig. 13 shows the control of the entire Green Power Inverter. The areas (in Fig. 13) enclosed by the hatched

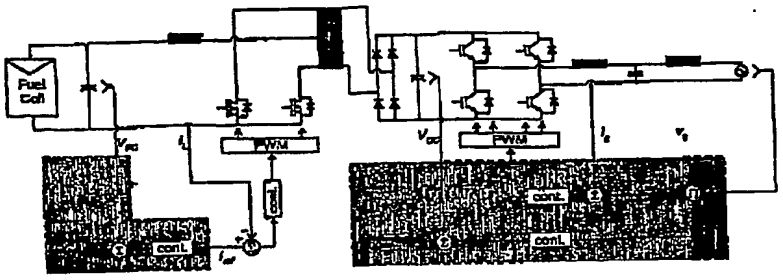


Fig. 13. System control of the green power inverter. (μP means controlled by micro-controller).

lines are implemented in a Siemens C167 microprocessor and hence, the control of the system is a mixture of digital and analog control. The fuel cell provides a reference for the fuel cell voltage V_{ref} and the GPI then controls the current reference in order to achieve the correct fuel cell voltage as the fuel cell follows a characteristic similar to Fig. 1. Since the dynamics of the fuel cell is very slow compared to the GPI capability a simple and slow search algorithm is implemented for the voltage control. The voltage control steps the current reference in accordance with the curve in fig. 1 towards the desired fuel cell voltage. It should be noted that the search algorithm does not need any information on the internal fuel cell resistance but only information of its maximum current and the operating voltage range of the fuel cell to avoid overloading the fuel cell. An analog PI-controller then controls the inductor current in accordance to the reference given by the micro controller through an D/A-converter.

The inverter control consist of two control loops. The inner control loop shapes the grid current to a waveshape proportional to the grid voltage. The outer control loop controls the amplitude of the grid current in order to maintain the average of the dc-voltage equal to the reference.

VI. Experimental results

Fig. 14 shows a picture of the tested GPI-converter. The DC-DC converter, the LCL-filter, the SMPS and all the control hardware have been designed, constructed and placed in the same box. The used inverter (VSI) is a commercial converter where all the control have been replaced in order to allow direct control of the IGBT switches via optical fibres.

Fig. 15 shows the performance of the inverter control in the whole power range. It is seen that the inverter exhibits a high power factor and a low current THD in practically the whole power range. The background distortion of the grid voltage was measured to THD_V=2.7% which also affects the final THD of the converter.

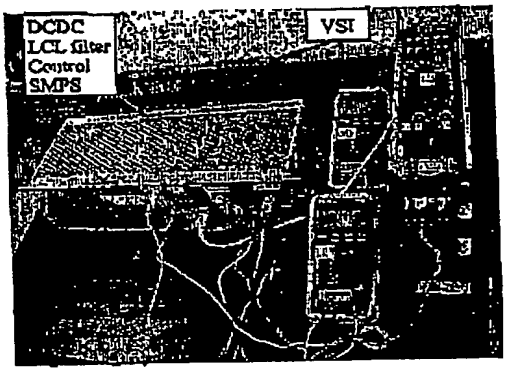
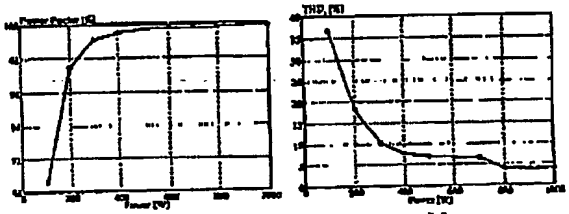


Fig. 14. Picture of the designed and implemented 1 kW GPI converter.

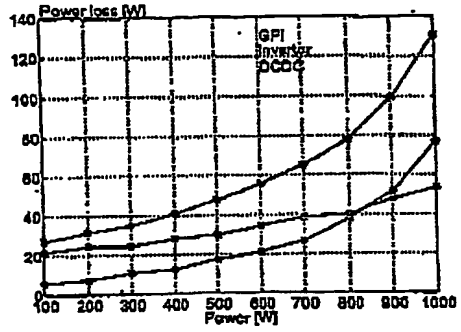


a) b)

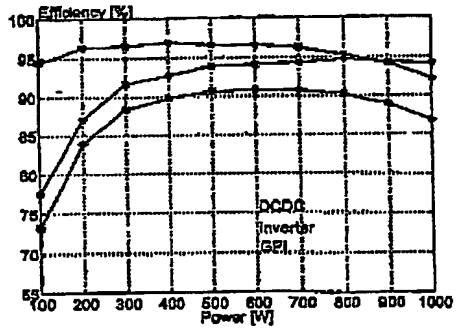
Fig. 15. Test of green power inverter. a) Power factor and b) current THD_I.

The losses and the efficiency of each part of the GPI system have been experimentally evaluated and they are shown in Fig. 16. It can be seen that the current fed push-pull converter (DCDC) exhibits a high efficiency in the whole power range but the inverter efficiency drops significantly in the low power range.

Fig. 17 shows a schematic of the units in the laboratory system and it can be observed that the used inverter includes an extra power supply (SMPS2).



a)



b)

Fig. 16. Measured overall GPI performance including VSI power supply. a) Power losses in system and b) efficiency.

The designed switched-mode power supply (SMPS) supplying the DC-DC converter is also intended to supply the control circuits of the inverter in the next generation of the green power inverter.

Fig. 18 shows the efficiency(top curve) when the measurements in Fig. 16 are compensated for the extra power consumption due to the VSI interior power supply(SMPS2). The lower curve is the direct measured efficiency and the middle curve shows the target efficiency of the GPI when the design and the development was initiated.

The system is tested on a real fuel cell. Fig. 19 shows a step response of the fuel cell voltage reference. The top curve shows the fuel cell voltage and the lower curve shows the grid current. The searching algorithm varies the current reference until the desired fuel cell voltage is reached. As expected the fuel cell voltage drops as the current increases (see Fig. 1). It is important that fault situations of the GPI does not damage the fuel cell. Therefore a sudden stop of the GPI was tested as shown in Fig. 20. The GPI input current drops suddenly to zero and the fuel cell voltage restores to the open circuit voltage as expected. Thus, a sudden stop of the GPI is handled safely by the fuel cell system.

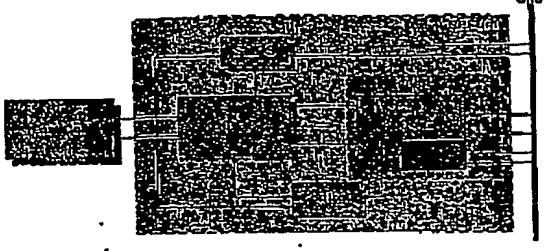


Fig. 17. Schematic of the implemented laboratory system.

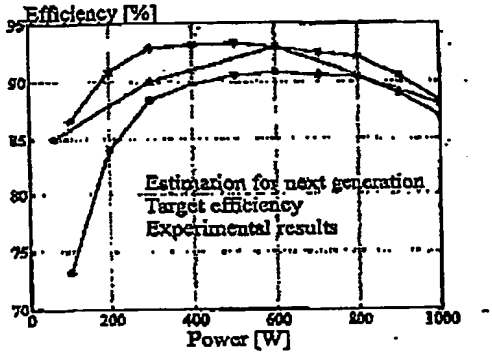


Fig. 18. Efficiency valuation and estimation for next generation of the green power inverter.

VII. Conclusion

This paper has presented a new green power inverter for fuel cells. The inverter has shown to be reliable and to exhibit a high efficiency in a wide input power range. The inverter exhibits a high power factor and a low current THD.

Experimental results verify the expected behaviour of the proposed green power converter. A soft startup procedure of the current fed push pull converter is developed and verified by experimental results.

The simplicity and the fact that the proposed converter is based upon well known technologies (ie. a commercial control IC exist for the converter, well known inverter and control of inverter) makes the proposed converter a potential low cost solution. The proposed green power inverter is believed to be a solution for fuel cell systems as well as photovoltaic cell systems due to its simplicity, high efficiency in a wide power range and low cost features.

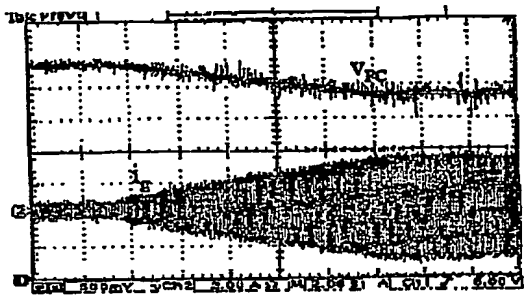


Fig. 19. Fuel cell voltage control. Top: fuel cell voltage, bottom: grid current.

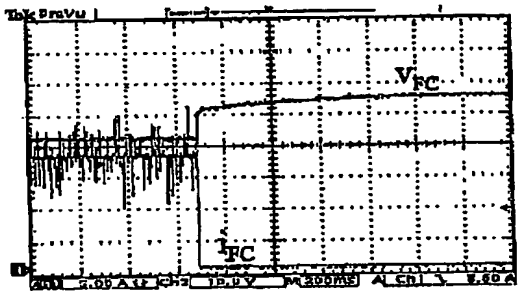


Fig. 20. Sudden stop of the GPI. The fuel cell current (green) decays to zero and the fuel cell voltage (blue) restores to open circuit voltage.

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Abstract— A full-bridge inverter for interfacing the utility grid is developed for using in a Green Power Inverter application. The inverter is feed from an arbitrary green power source (fuel cell, photovoltaic, small wind turbine etc.) through a rectifier into the dc-link. In order to maintain a sinusoidal grid current with low harmonic distortion and a high power factor, the inverter is controlled to emulate a negative resistance towards the grid. The size of the emulated resistor is determined by the dc-link voltage controller, which tries to maintain a constant dc-link voltage. This is however not possible, while the power into the dc-link is constant and the power out of the dc-link is a second powered sinusoidal with an amplitude of two times the average power. For that reason a small ripple is present. In order to lower the transmitted high frequency current ripple, due to the operation of the inverter, a LCL filter is inserted between the grid and the inverter. It is shown that the LCL filter may be regarded as an inductor for frequencies slightly below the filters resonant frequency; hance the control of the filter becomes easy. On the other side, the z-plane poles for the filter, even with parasitic resistances, lie close to the border of the unit-circle. Adding a resistance in parallel with the outer inductor in the LCL filter shows to improve the stability on the cost of a little higher loss. A 1 kW Green Power Inverter was designed and implemented in the laboratory. The result shows that the LCL filter is stable when the damping-resistor is added. The total harmonic current distortion was measured below 4,0 the power factor is better than 0,99 for an input power above 300 W.

I. Introduction

GREEN POWER -also known as renewable power, becomes more and more visible when seeking new solutions for the worlds still increasing power demand. The major contribution from the green power sources today is the hydropower, which contributes with one fifth of the worlds total power generation [1]. Another great player among these sources are the wind turbines. In Europe alone there is an accumulated installed power of 13 000 MW [2], which is capable of delivering power to 7 million citizens. Other types of green power sources are the photovoltaic cell [3], the fuel cell and the sea-wave sources. On the other hand, the fuel cell may not be a direct source to green power because it need fuel e.g. hydrogen, methane or other high-level hydrogen-carbon compounds. The fuel-cell system could instead be used as an energy-buffer when the generation from the other green power sources does not fit the actual power demands.

This paper addresses some aspects of controlling a grid-connected green power inverter, such as designing the control strategies for the LCL filter and inverter [4], [5], [6].

The topology for a Green Power Inverter is presented in section II. The topology includes a full-bridge inverter together with a LCL filter towards to utility-grid. Section III deals with the control of the system. The control loops includes a controller for the grid current and the dc-link voltage. It becomes in this way possible to attach more that one power source to the same inverter-stage. Some experimental results are presented in section IV and a conclusion is given in V.

II. Topology

The system is made up around an inverter and the LCL filter, see Figure 1.

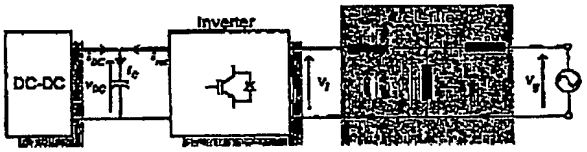


Fig. 1. Line filter configuration together with inverter and grid.

The LCL filter has the following components:

$$Z_i = R_i + L_i s \quad (1)$$

$$Z_g = R_g + L_g s \quad (2)$$

$$Z_0 = \frac{1}{Cs} \quad (3)$$

And the component values are listed in Table 1, cf. [4]. In the general case all passive elements are treated as impedances.

$$V_i = (Z_i + Z_0)I_i - Z_0 I_g \quad (4)$$

$$V_g = Z_0 I_i - (Z_0 + Z_g)I_g \quad (5)$$

$$I_i = \frac{Z_0 + Z_g}{Z_0} I_g + \frac{1}{Z_0} V_g \quad (6)$$

$$I_g = \frac{Z_0}{Z_g + Z_0} I_i + \frac{-1}{Z_g + Z_0} V_g \quad (7)$$

After some manipulation of equations (4) to (7) the following transfer functions appears

$$H_{i\to g}(s) = \frac{I_g(s)}{V_i(s)} = \frac{Z_0}{Z_0(Z_i+Z_g)+Z_iZ_g} \quad (8)$$

$$H_{i\to i}(s) = \frac{I_g(s)}{V_i(s)} = \frac{Z_0+Z_i}{Z_0(Z_i+Z_g)+Z_iZ_g} \quad (9)$$

$$H_{g\to g}(s) = \frac{I_g(s)}{V_i(s)} = \frac{Z_0+Z_g}{Z_0(Z_i+Z_g)+Z_iZ_g} \quad (10)$$

$$H_{g\to i}(s) = \frac{I_g(s)}{V_i(s)} = \frac{-Z_0}{Z_0(Z_i+Z_g)+Z_iZ_g} \quad (11)$$

These are the four transfer functions linking the two filter terminal voltages (grid voltage and inverter voltage) to the corresponding inductor currents. For the purpose of control the transfer functions of interest are $H_{i\to g}(s)$ and $H_{i\to i}(s)$.

Figure 2 shows the amplitude responses when parasitic conducting resistance is included. Figure 2.b shows a comparison between each of the amplitude responses with and without parasitic conducting resistance. Damping of the filter can be utilized in order to improve the stability of the current loop. This will be treated in the next section. Filter transfer functions are derived when passive damping of the outer inductor is introduced. The damping is introduced by adding a resistor in parallel with the inductor towards the grid.

$$Z_g = L_g s \| R_d = \frac{L_g s R_d}{L_g s + R_d} \quad (12)$$

TABLE I
LINE FILTER PARAMETERS. R_i AND R_g ARE DC-VALUES.

L_i [mH]	R_i [mΩ]	L_g [μH]	R_g [mΩ]	C [μF]
4.0	400	850	180	2.2

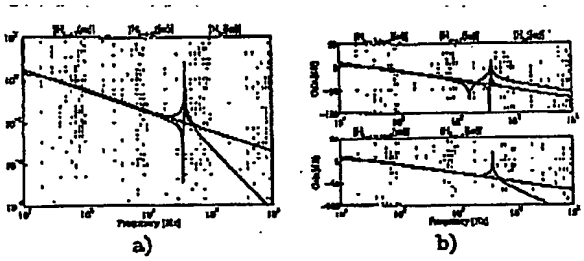


Fig. 2. Amplitude response of LCL filter. a) Comparison of the different transfer functions. It is seen that the LCL filter has a $H_{L\to g}(s)$ frequency response (The inverter voltage to grid current) equal to the LR filter for frequencies slightly below the resonant frequency. b) Comparison between the ideal cases without series conduction resistance and the non-ideal case including these resistors.

Transfer functions have been derived for the LCL filter for the purpose of current control. A comparison between these third order functions and a inductive equivalent shows that below the resonance frequency the single inductor-resistor equivalent is an adequate approximation of the inverter voltage to inverter current but in order to describe/analyse stability the LR circuit is not adequate near the resonance frequency of the LCL filter.

III. SYSTEM CONTROL

The aim of the inverter control is to load the DC-link capacitor in order to maintain the dc-component of the link voltage at the desired value $V_{dc,ref}$. The current impressed into the utility grid must comply with EMC regulations. In addition, the inverter must be fast enough to protect the dc-link and the semiconductors from over voltages due to power processing from the power source.

Besides the harmonic content of the line current, two performance indexes are used: $\%THD_I$ and PF. With perfect resistor emulation and with a background distorted line voltage, the line current $\%THD_I$ will be the same as the line voltage distortion $\%THD_V$. The power factor will be unity for perfect resistor emulation and regardless of background distortion.

A. Grid-Current Control

There exist several methods/strategies to control the grid-connected inverter. In order to fulfil the low harmonic regulation IEC 61000-3-2, the innverter is controlled to emulate a resistor R_e. Hence, the grid current waveform must be a scalar of the voltage waveform: $R_e = v_g/i_g$. Figure 3 shows the control principle of the grid-current and dc-link voltage.

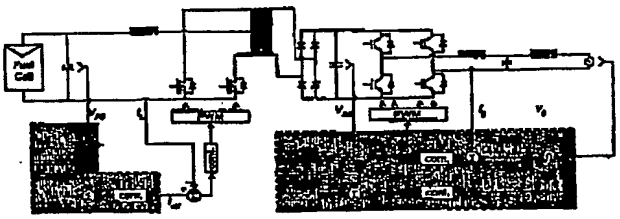


Fig. 3. Control strategy of the whole GPI converter.

The inner current loop shapes the line current to a shape similar to the line voltage. The outer loop controls the dc-link voltage. Hence, the inverter emulates a resistance by means of two cascaded loops. The grid and the inductor current are not sinusoidal because the dc-link voltage control loop distorts the current reference, which the current controller follows (cf. the multiplier in Figure 3). For that reason, the sampling time of the dc-link voltage controller should be equal to 20 ms. The dc-current injection to the grid is in this way reduced to a minimum.

Figure 4 shows the block diagram of the current control loop. The input reference is the inverse of the emulated resistance $R_e(z)$. The emulated conductance $G_e(z) = R_e^{-1}(z)$ is multiplied with the grid voltage in order to form the current reference. The voltage generated by the inverter $V_i(s)$ to the system $H_{i\to i}(s)$ is the sum of the current

controller $D(z)$ and the feed-forward of the grid voltage $V_g(z)$. Figure 2.a reveals that at frequencies well below the filter resonance frequency then $|H_{i\to g}(jw)| \approx |H_{i\to i}(jw)|$ which is also true for the phase margin. Thus, a feed-forward of the grid voltage cancels the influence from the grid voltage (at low frequencies). But it is also obvious that the feed-forward loop has less attenuation at higher frequencies and is thus not immune towards high frequency noise. Therefore a low-pass filtering of the feed-forward loop should be used in order to avoid noise problems.

Design of the current controller will be done based on both the third order LCL transfer function and on the simple LR model.

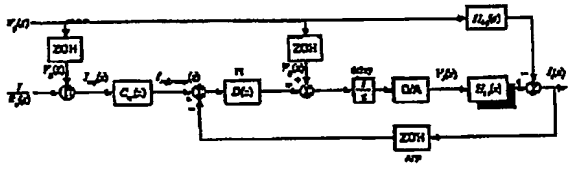


Fig. 4. Control block diagram for the current loop.

In order to obtain a high PF and a low $\%THD_I$ the current controller must be able to track not only the fundamental grid frequency at 50 Hz but also the distortion components. The switching frequency and the sampling frequency is 10 kHz. In order to handle background distortion the settling time of the current controller is set to $X = 10$ samples witch yields 1 ms. Setting the damping ratio to $\zeta = 1/\sqrt{2} \approx 0,707$ provides optimal step response in terms of settling time and over shoot. Hence the desired placement of the dominating poles is

$$s_{1,2} = \zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2} \approx 4440(-1 \pm j) \quad (13)$$

$$z_{1,2} = exp(T_s s_{1,2}) = \approx 0,579 \pm j0,276 \quad (14)$$

Hence, a natural frequency at $\omega_n = 2\pi/(XT_s) = 6283$ rad/s is obtained.

Ideally, the current controller must be able to follow a sine wave as reference. If it is regarded as a ramp reference signal then system must be at least a type 2 in order to have zero steady state error. A type 1 system will have a finite error. Since the filter is a type 0 system, two additional integrators must be added which in terms of stability is very difficult to handle. While the settling time is much lower than then grid periode the system can be treated as operating in quasi steady state with step inputs. A type 1 system have zero steady state error towards step input reference signals, therefore:

- PI controller is selected as current controller.
- The PI current controller will have a finite steady state error which decreases as the proportional gain increases.
- Roughly, the integrational part determines the phase shift between the grid voltage and current, and the proportional gain determines the reference signal tracking ability.

The discrete transfer function of the $L_i s + R_i$ impedance is

$$H_{ir}(s) = \frac{1}{L_i s + R_i} = \frac{1}{R_i}\frac{R_i/L_i}{s + R_i/L_i} \quad (15)$$

$$H_{ir}(z) = \frac{z-1}{z} Z\left(\frac{H_{ir}(s)}{s}\right) = \frac{1-\alpha}{R_i}\frac{1}{z-\alpha} \quad (16)$$

where $\alpha = exp(-R_i/L_i T_s)$. The PI controller transfer function is given as:

$$D(z) = K_p\frac{z(1+T_s/T_i)-1}{z-1} \quad (17)$$

The open loop grid current transfer function including delay:

$$H_{ir}(z)D(z)\frac{1}{z} = K_p\frac{1-\alpha}{R_i}\frac{z(1+T_s/T_i)-1}{z^3-(1+\alpha)z^2+\alpha z} \quad (18)$$

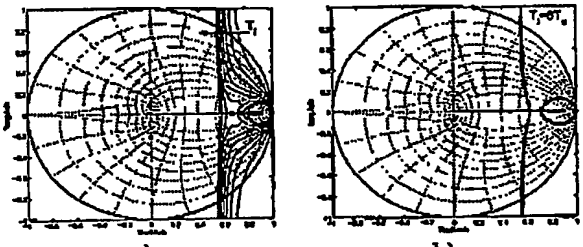
Figure 5.a shows the influence on the root locus when the integration time T_i varies. In order to have a locus passing the desired pole placements an integration time $T_i = 8T_s$ have been chosen. Figure 5.b shows the root locus for $T_i = 8T_s$.

At a proportional gain at $K_p = 14$ the poles and zeros of the closed loop is listed in Table 2. Figure 6.a shows the step response of the current control system (blue) and the desired step response (red). The dynamics are a bit different to the specified performance due the extra pole added from the unit delay. The real pole and the real zero can be compensated in order to make the dynamics match the specifications:

TABLE II

SYSTEM POLES AND ZEROS OF THE CURRENT CONTROL LOOP.

Poles	Zeros	K_p	T_i/T_s
0.8333	0.8889	14	8
$0.5784 \pm j0.2888$			

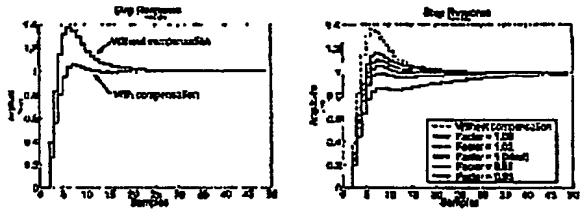


a) b)

Fig. 5. Root locus of current loop including delay. a) Different integration times and b) root locus at $T_i = 8T_s$.

$$G_{zp}(z) = \frac{1-n}{1-p}\frac{z-p}{z-n} = K_c\frac{1-nz^{-1}}{1-pz^{-1}} \quad (19)$$

Figure 6.b shows the step response with compensation but also the effect of not compensating correctly. Thus in order to utilize compensation it is required to match the system poles and zeros exactly.



a) b)

Fig. 6. Step response of current loop. a) with and without compensation and b)robustness of the compensation accuracy.

Analysing stability of the current loop with the third order LCL model it is necessary to include damping or some equivalent manipulation of the open loop poles at unity proportional gain. Here passive damping with a resistor in parallel with the grid-connected inductor is used.

Figure 7.a shows open loop poles and zeros without (black) damping and the system poles (red) and zeros (blue) with different damping values. Of course as the damping resistor increases the poles and zeros moves towards the un-damped positions. It can be observed that the open loop poles without damping are placed very close to the border of stability. Using Figure 7.a alone it would be reasonable to choose the damping resistor as low as possible. But since the power dissipation in the damping resistor increases and filter attenuation decreases, as the resistor value decreases there exist a trade off between stability, efficiency and filter attenuation. A damping resistor at $R_d = 38\ \Omega$ has been chosen and will be used throughout this paper.

B. dc-link voltage controller

Varying the amplitude of the grid current i_g controls the dc-link voltage. The dc-link voltage must be maintained on a level above the peak of the line current in order to be able to maintain controlability of the inverter. The dynamics of the current loop will be neglected during design of the voltage controller since the current loop bandwidth is app. 250 times higher than the outer voltage loop bandwidth.

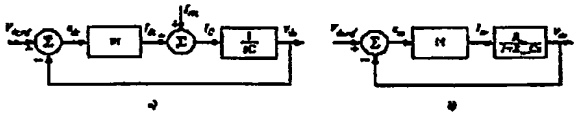
The trade off gives a very slow dc-link control and a sampling time equal to $1/f_{grid}$. Setting again the damping ratio to $\zeta = 1/\sqrt{2} \approx 0,707$ and taking the slow dynamic operational requirements into account the bandwidth of the voltage controller can be chosen very low around $f_{b,dc} =$ 2...5 Hz. Letting the settling time to 2500 samples and ω_n = 25 rad/s (4 Hz) together with (13) and (14) yields the desired pole placement of the voltage control loop: $z_{1,2} = 0,9982 \pm j0,0018$

Figure 1 shows a diagram of how the dc-link interconnects the DC-DC converter and the DC-AC inverter.

For perfect resistor emulation and with sinusoidal grid voltage the power balance gives:

$$< i_{dc} >_{t_g} = \frac{\hat{i}_g \hat{v}_g}{2 < v_{dc} >_{t_g}} \qquad (20)$$

Thus in steady state there is a simple relation between the dc current and grid current. A PI controller is selected in order to achieve a dc voltage error at zero and to have a more smooth dc current reference less sensitive to noise. Figure 8.a shows the block diagram of the dc-link control of the circuit in Figure 1 where the rectified current is treated as a disturbance since this parameter is not measured. Making a linear approximation around an operating point of rectified current gives the block diagram in Figure 8.b where the resistance $R_{rec} = V_{DC}/I_{rec}$.



a) b)

Fig. 8. Equivalent circuit for dc-link control.

At full load the input power is 1 kW and the dc voltage is 375 V which gives the minimum resistance$(375\ V)^2/1\ kW = 141\ \Omega$. The transfer system transfer function for the voltage control loop then becomes:

$$H_{dc}(s) = \frac{V_{dc}(s)}{I_{dc}(s)} = \frac{1}{sC_{dc}} || R_{rec} \qquad (21)$$

$$H_{dc}(z) = \frac{z-1}{z} Z\left(\frac{H_{dc}(s)}{s}\right) = \frac{R_{rec}(1-\beta)}{z-\beta} \qquad (22)$$

where $\beta = exp(-T_s/R_{rec}C)$. The PI controller is given in (18). The open loop dc-link voltage transfer function including delay:

$$H_{dc}(z)D(z)\frac{1}{z} = K_p R_{rec}(1-\beta)\frac{z(1+T_s/T_i)-1}{z^3-(1+\beta)z^2+\beta z} \qquad (23)$$

Figure 9 shows the influence in the root locus by varying the integration time. At a proportional gain at K_p = 0.0166 the poles and zeros of the closed loop are listed in Table 3. Figure 10.a shows step the response of the existing control system (blue) and the desired step response (red). The dynamics are a bit different to the specified performance due the extra pole added from the unit delay. Again, the real pole and the real zero can be compensated in order to make the dynamics match the specifications.

IV. EXPERIMENTAL RESULTS

This section evaluates the performance of the first Green Power Inverter prototype. The grid-connected inverter is made up around a full-bridge inverter, in this case a modified Danfoss VLT 5001 frequency converter and the LCL filter, see also Figure 1. The VLT 5001 is modified in order to get direct access to the dc-link and a IPC-VLT500 Interface and Protection Card [4] is included in order to protect

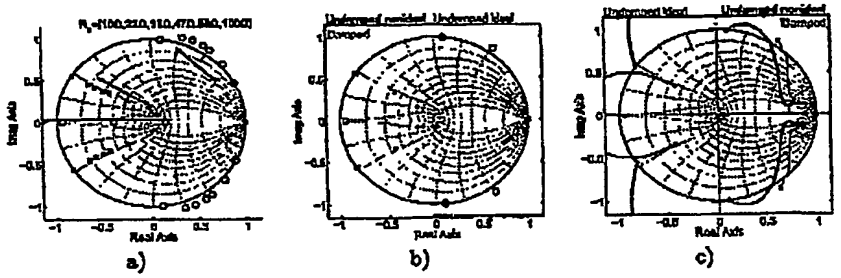


Fig. 7. Effects on open loop poles when passive adding damping. a) Different damping resistors, b) $R_d = 38\ \Omega$ and c) root locus with and without damping resistor (38 Ω).

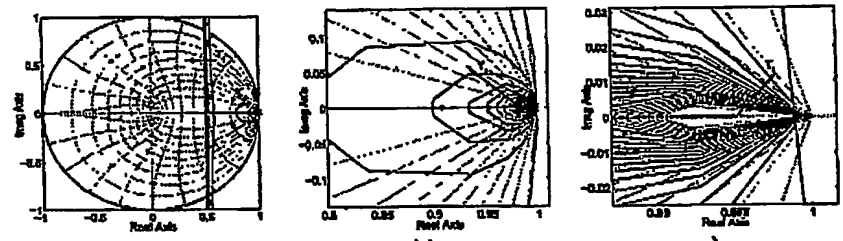


Fig. 9. Root locus of voltage loop including delay. a) Different integration times, b) a zoomed view and c) a zoomed view near the desired pole placements.

TABLE III
SYSTEM POLES AND ZEROS OF THE VOLTAGE CONTROL LOOP.

Poles	Zeros	K_p	T_i/T_s
0.0025 0.9982 ±j0.0018	0.9975	0.0166	400

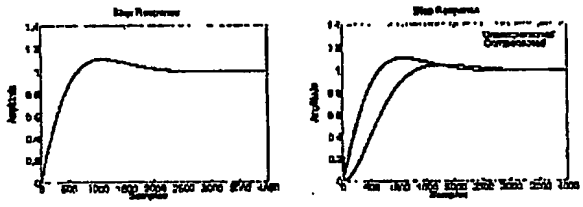


Fig. 10. a) Step response of designed voltage loop and b) including compensation.

and control the frequency converter. Figure 11 shows the grid current and grid voltage at 600 W and 1000 W respectively. This figure illustrates the resistor emulation as the grid current and voltage is in phase and the wave shapes are alike. There are some high frequency oscillations in the grid current at the switching frequency. These oscillations are due to noise in the feedback in the prototype. Figure 12 shows the grid performance of the GPI in terms of power factor and $\%THD_I$.

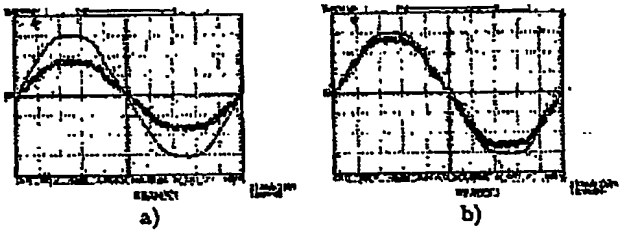
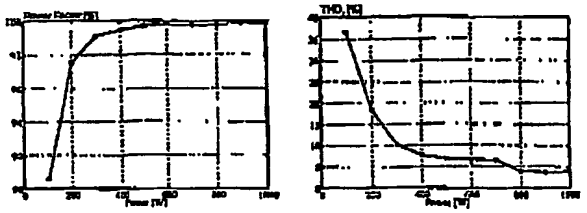


Fig. 11. Grid current at a) 600 W and b) 1000 W.

V. CONCLUSION

This paper presented some aspects of controlling the Green Power Inverter interface towards the grid. In can be concluded that the LCL filter is a good choice for lowering the harmonics to the grid. However, the poles for the undamped LCL filter lies close to the border of the unity circle and something must be done in order to increase stability. The stability may be increased by adding a resistance in parallel with the inductor towards the grid. Next was the grid-current loop investigated and designed in z-plane for the proposed LCL filter. The inherent unit delay from the micro processor was dealt with by adding a proper compensation. The designed controllers followed



a) b)

Fig. 12. Power factor and total harmonic distortion in the grid current. The background $\%THD_V$ was measured to 3% so the minimum $\%THD_I$ is also 3% .

the given specifications. In order to control the dc-link voltage, a PI controller was included in the design. The output from the PI controller is multiplied with the grid-voltage, in order to generate the current reference for the inner-loop. The inverter operates in this way like a resistance toward the grid and low a $\%THD_I$ and a high PF should be reachable.

Root locus analysis reveals that the designed controllers are robust in means of stability and accuracy. Measurements in the laboratory reveals that the designed and implemented controllers reacts as specified. A total harmonic current distortion of 3,8 % is obtained when a background voltage distortion of 3,0 % is present. The power factor is better the 0,99 for power levels above 300 W.

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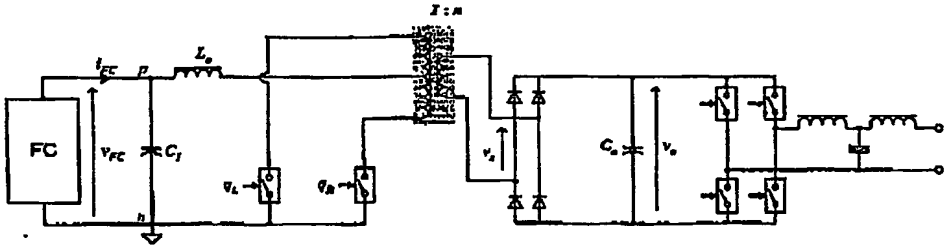


Figure 1.15: *CSVS-Push pull converter.*

Power [W]	Voltage [V]	Current [A]	$\frac{V_{FC}}{V_{DC}}$	D
60	53.6	1.12	0.1428	0.7858
300	47	6.38	0.1253	0.812
600	30	20	0.0800	0.88
1150	25	46	0.0667	0.90

Table 1.7: *Characteristic values for the CF-Push-Pull GPI in the four specified operating points.* $D_{max} = 0.9$ *and* $n_{min} = 1.5$.

The Current-Fed Push Pull DC-DC converter (SIC)

Shown in Fig. 1.15, the current fed push-pull do-dc converter is a isolated boost converter. The steady state transfer functions are:

$$\frac{v_o}{v_{FC}} = n \cdot \frac{1}{1-D} \qquad \text{and} \qquad \frac{i_{L_o}}{i_{FC}} = \frac{1-D}{n} \tag{1.16}$$

Advantages:

- High efficiency.
- Well known technology.
- Bidirectional magnetisation of the transformer.
- Low transformer ratio.
- Low ripple in input current.

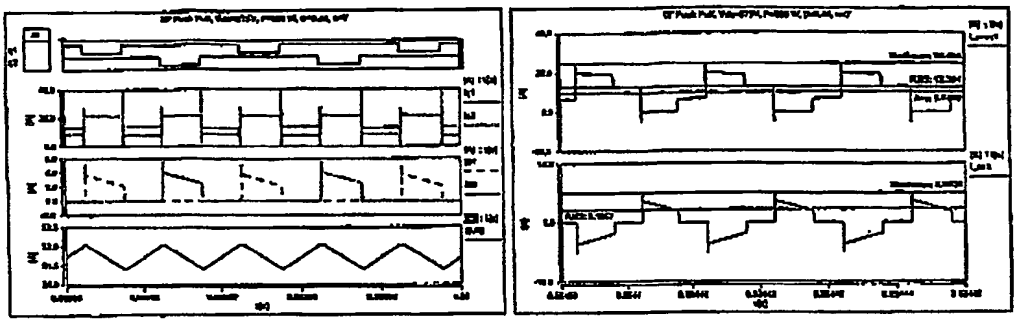


Figure 1.16: CF Push pull converter at $D = 0.45$, $R_L = 234\Omega$

Feature	Value	Unit
$i_{Q,rms}$	12.57	A
$i_{Q,av}$	9.90	A
$i_{D,rms}$	1.48	A
$i_{D,av}$	0.76	A
$i_{Trafo,prim,rms}$	12.39	A
$i_{Trafo,sek,rms}$	2.14	A

Table 1.8: *Characteristic values for the CF-Push-Pull GPI at 600W.* $D_{max} = 0.44$ *and* $n = 7$.

Drawbacks:

- High output voltage ripple.
- High voltage across the main switches - twice the output voltage referred to the primary.

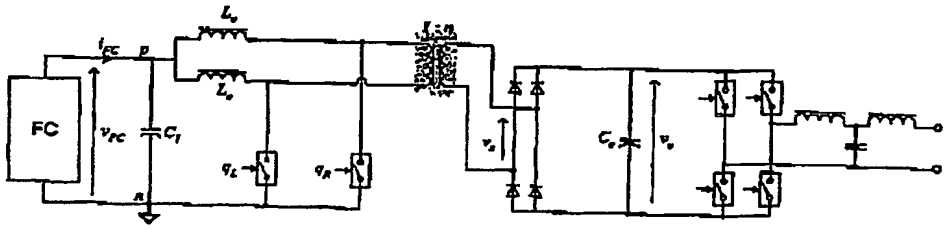


Figure 1.17: *DIC-Push pull converter.*

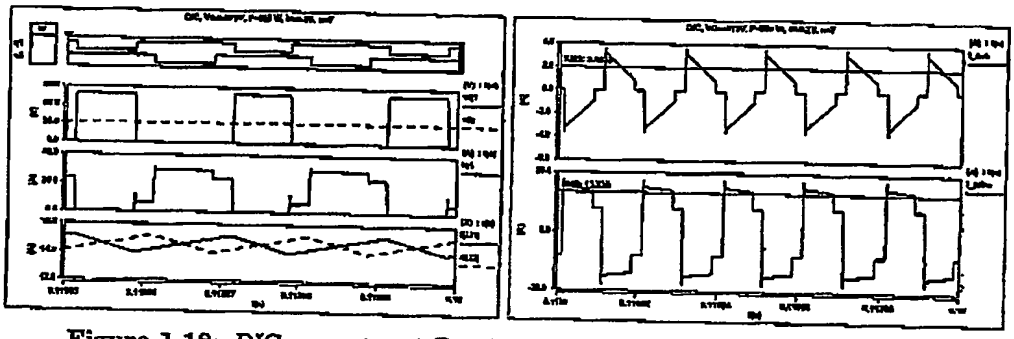


Figure 1.18: *DIC converter at* $D = 0.25$, $R_L = 234\Omega$

The Dual Inductor Voltage Source Push Pull based converter (DIC)

Shown in Fig. 1.17.
Compared with the SIC converter the DIC has the following advantages

Advantages:

- Low total inductor volume.
- Lower input current ripple.

1.4.3 Dual full bridge converters

This section is devoted to the investigation of the losses and ratings in the three dual full bridge topologies. The three solutions are based on a voltage source inverter connected to the grid, fed from a dc/dc converter. The dc/dc converter topologies are based on three different methods: the Voltage Source Converter, the Current Source Converter and the

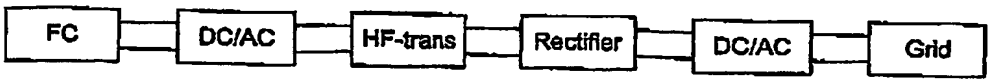


Figure 1.19: *System overview.*

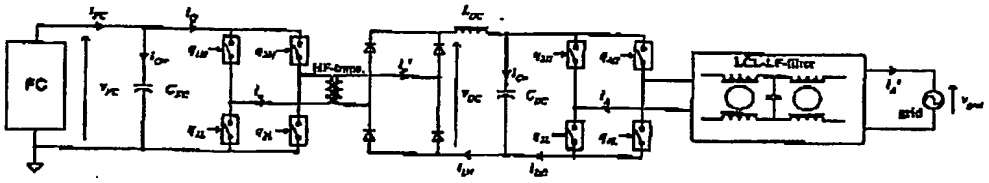


Figure 1.20: *The Voltage Source-Voltage Source Topology.*

Active Clamped Current Source Converter. The fundamental operation of the dual full bridge topology is as given, with refer to Fig 1.19: The voltage delivered by the Fuel Cell is inverted to a high frequency voltage in the first DC/AC inverter. This voltage is feed into the high frequency transformer. The transformer secondary turns is connected to a rectifier with a filter, and thereby is the DC/DC converter achieved. The voltage delivered by the DC/DC converter is fed into the DC/AC inverter, whose mains task is to generate a sinusiodal grid current.
The DC/DC converter is controlled in such a way, that the current delivered by the FC is constant at the desired value. This may cause the voltage of the dC-link between the rectifier and DC/AC inverter to rise beyond a certain limit. Therefore, the DC/AC inverter is controlled to lower the dc-link voltage, meanwhile it also generates the grid current. This means that the reference for the peak grid current is dictated by the maximum dc-link voltage.
The advantages of these two stages inverters are that the energy storage capacitors may be reduced in size, when compared with the single step topologies. It may also be easier to obtain a controller for these inverters, because they are decoupled by the energy storage. Moreover, they all utilize a HF transformer, which is much smaller then a 50 *Hz* transformer, for the galvanic isolation and stepping up the FC voltage.
The largest disadvantages is the efficiency, which is believed to fall, because of the extra power devises.

1.4.4 Voltage Source - Voltage Source

The Voltage Source - Voltage Source converter is depicted in Fig. 1.20, and the key waveforms in Fig. 1.21. The converter is based on a proven technology, and may therefore be more reliable then the solution presented in the following section. The two major disadvan-

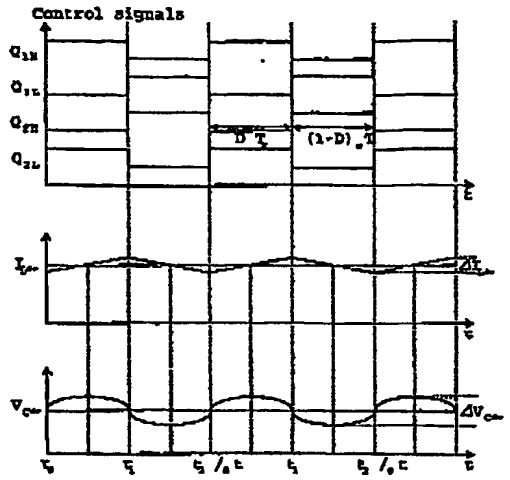


Figure 1.21: *VSVS Converter waveforms.*

tages are than the converter is based on the principle of buck operation, which means that it is not possible to step up the voltage without the transformer. Hence, the turn ratio is stated in the light of the minimum FC voltage and the corresponding duty cycle. This may cause the transient voltage on the secondary side of the transformer to raise beyond 1 kV when the converter is operated at its nominal point. The other disadvantages, is that the diodes in the rectifier is forced to commutate by a voltage, which generates reverse recovery currents.

Mode of Operation

[$t_0 \rightarrow t_1$] Transistors Q_{1H} and Q_{2L} are on, causing the transformer current i_a to be negative. The applied, negative, voltage on the primary side is reflected to the secondary side, with a gain of n, which is the turns ratio. The voltage difference between the transformer and the dc-link capacitor C_{DC} causes an increase in the inductor current, inductor L_{DC}, which feeds the load. The current ripple is bypassed by the dc-link capacitor, and the dc/ac inverter is therefore not exposed to any HF current, originated from the dc/dc converter.

[$t_1 \rightarrow t_2$] Transistors Q_{1L} and Q_{2H} are on, and the transformer is now forward biased.

The steady state voltage transfer function is given by

$$\frac{V_{DC}}{V_{FC}} = n \cdot D \tag{1.17}$$

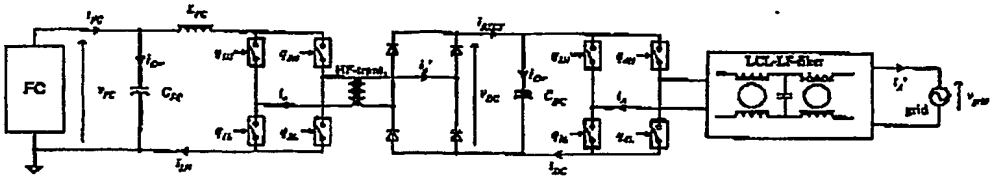


Figure 1.22: *The Current Source-Voltage Source Topology.*

where D is the duty cycle, see Fig. 1.21 for the definition of D, and n is the transformer turns ratio.

1.4.5 Current Source - Voltage Source

The Current Source - Voltage Source converter is depicted in Fig. 1.22, and the key waveforms in Fig. 1.23. The converter is based on a proven technology, but is it seldom used in the low power region. The major advantages are than the converter is based on the principle of flyback operation, which means that it is possible to step up the voltage without the transformer. The other advantages, is that the diodes in the rectifier is commutate by a current, and no reverse recovery currents are therefore generated. As far as we can seen at this point of view, the only disadvantages associated with this converter, is the inherent presence of voltage spikes across the switches. These spikes originates from the transformer current and leakage inductance. In practice, the leakage inductance may be made small by making a proper transformer design, but not small enough in order to omit a passive and lossy snubber. The passive snubber may reduce the overall efficiency, and should therefore be avoided.

Mode of Operation

$[t_0 \rightarrow t_1]$ All four switches is closed, causing the inductor current $i_{L_{FC}}$ to rise linear, by means of the cell voltage. The inductor current is given in Eq. (1.19). The cell voltage is clamped by the input capacitor C_{FC}, so only a little amount of ripple is present. The output is supplied by the stored energy in C_{DC}

$[t_1 \rightarrow t_2]$ The transistors Q_{1L} and Q_{2H} turns off at time t_1. The current stored in the input inductor is then forced through the transformer, and the inductor is discharged by means of the cell voltage and the reflected dc-link voltage, given by Eq. (1.20). The transformer current i_a is negative, and feeds the output capacitor C_{DC} through the rectifier.

$[t_2 \rightarrow t_3]$ Transistors Q_{1L} and Q_{2H} turns on again at time t_2, and the input inductor is charged again.

Circuit diagram of PV Inverter
Dc-dc and grid inverter

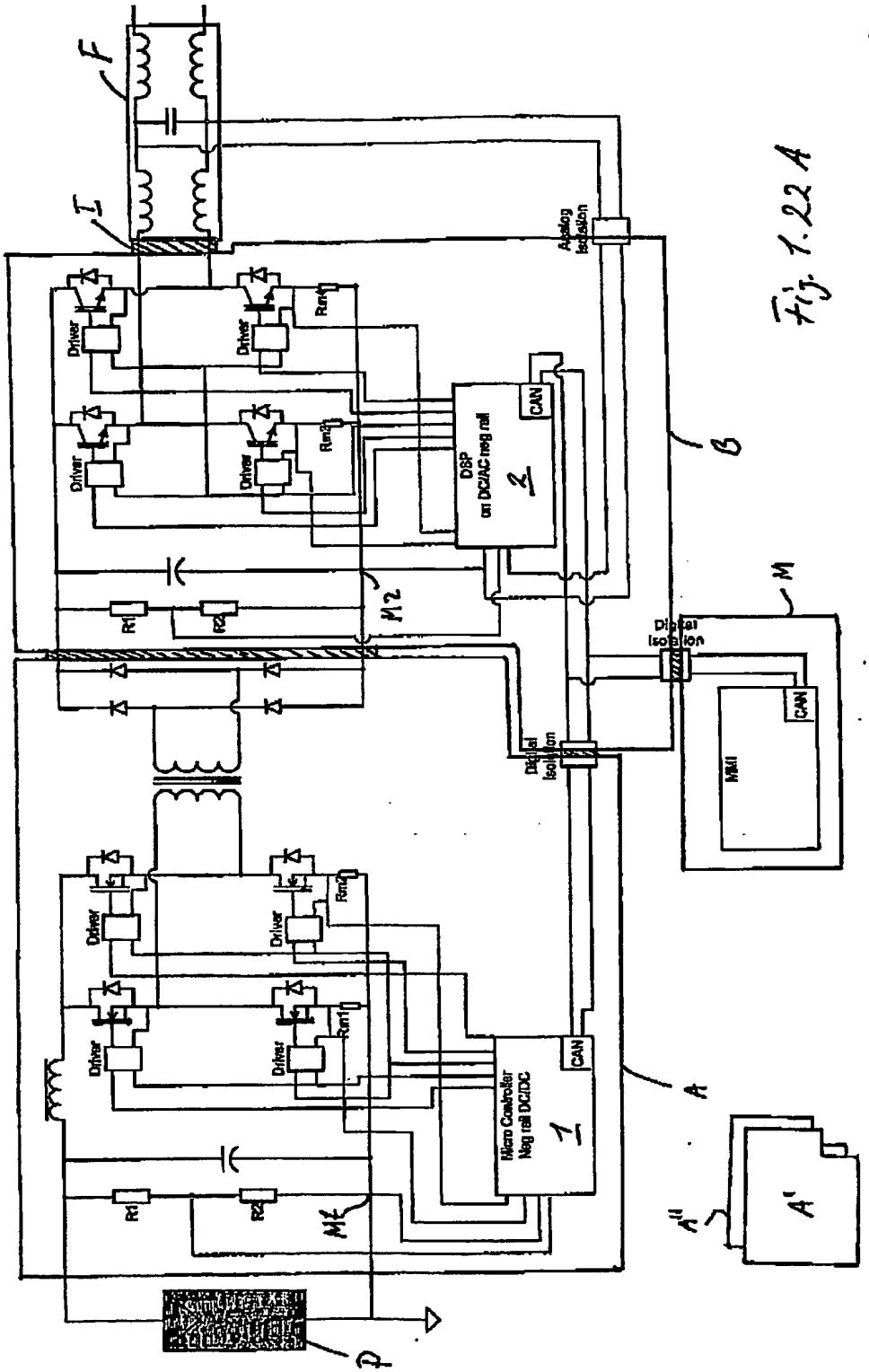


Fig. 1.22 A

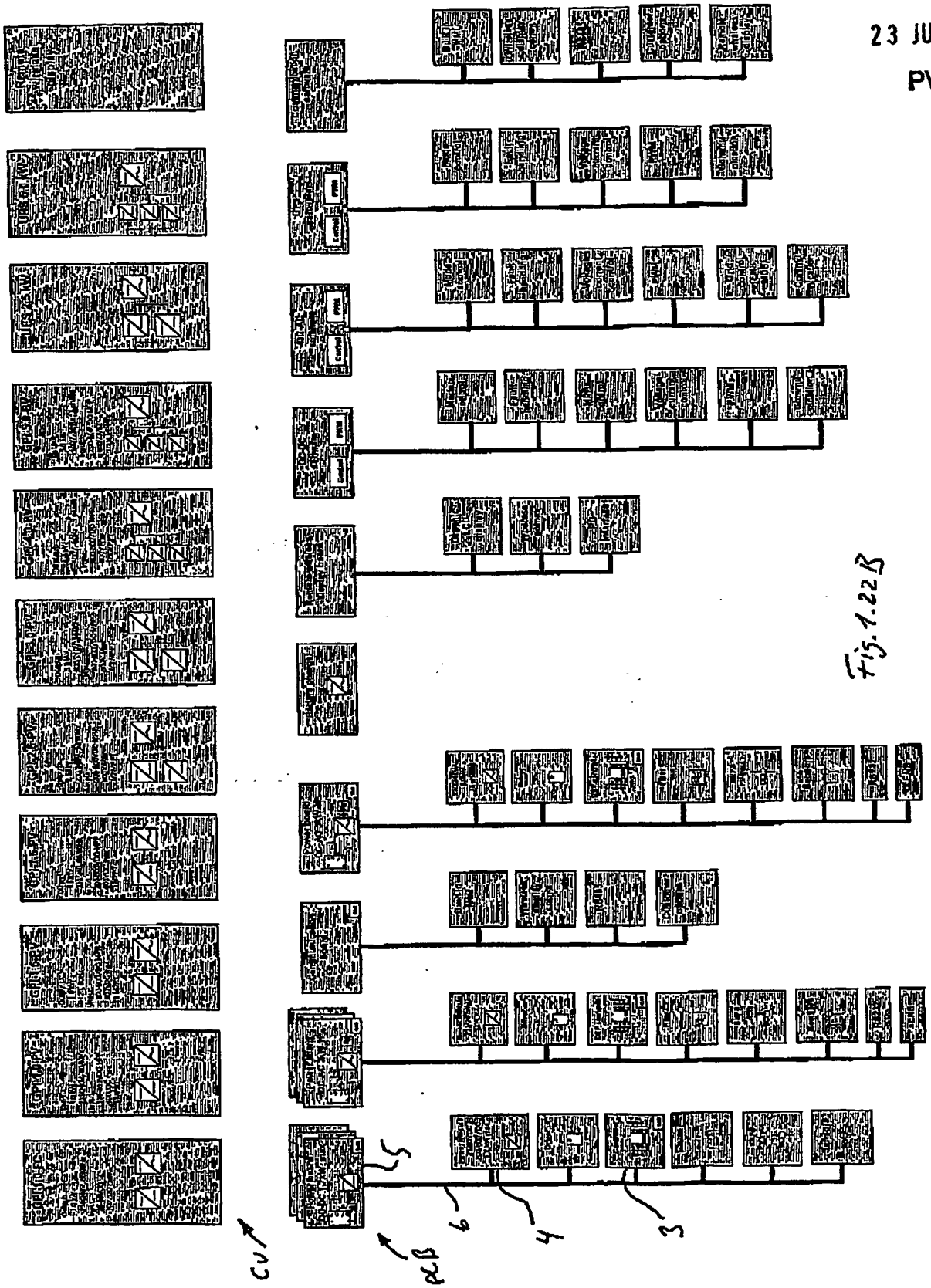


Fig. 1.22B

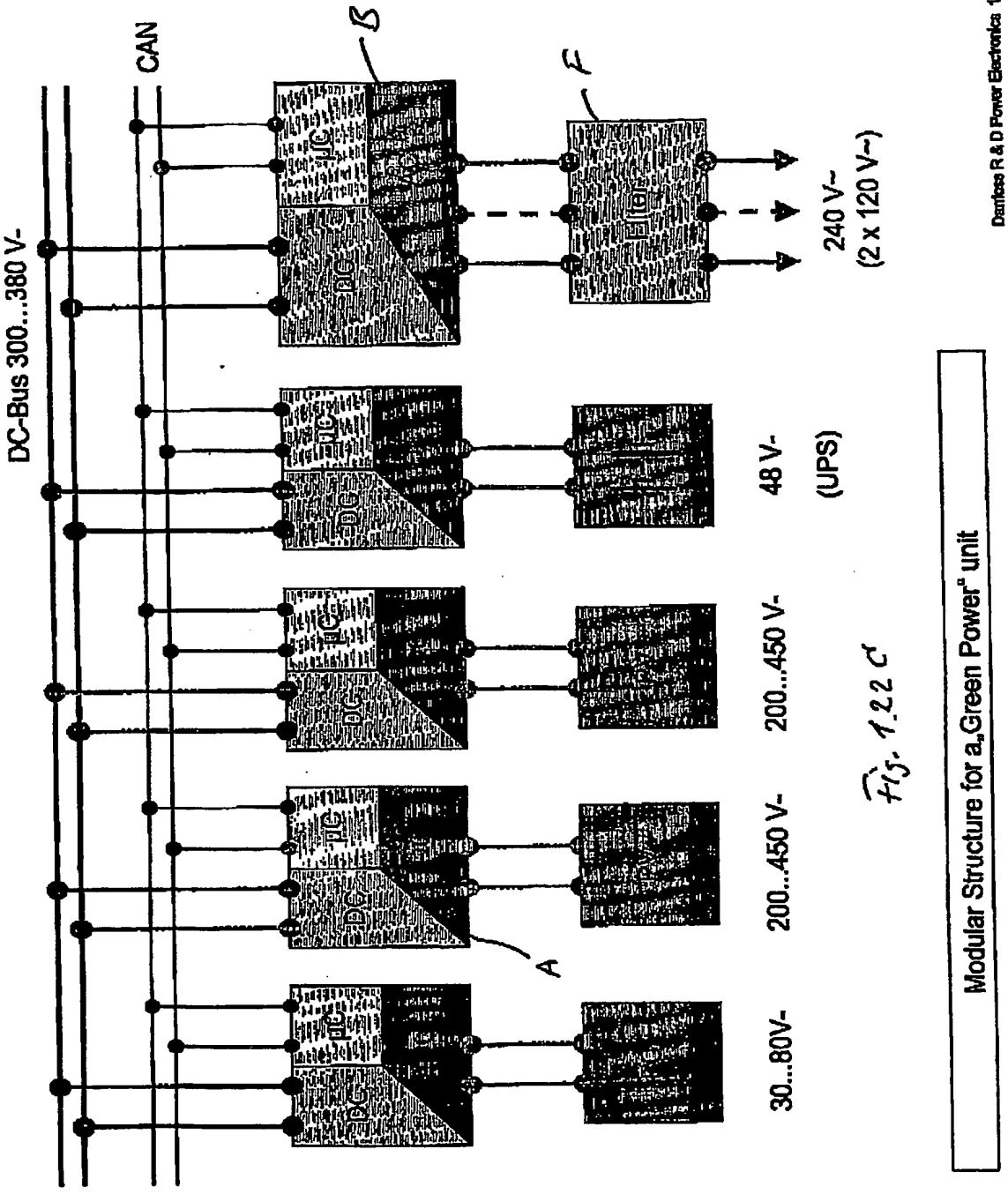


Fig. 1.22 c'

Modular Structure for a „Green Power" unit

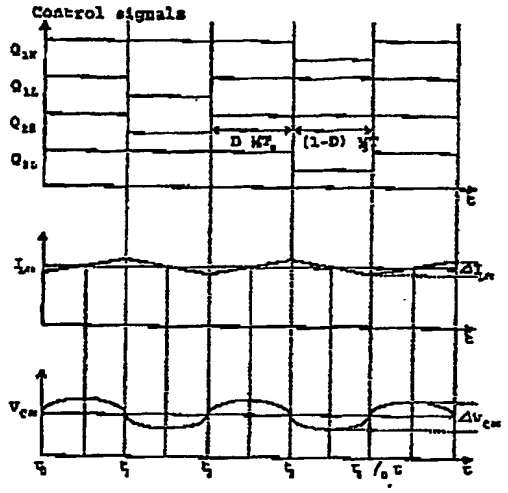


Figure 1.23: *CSVS Converter waveforms.*

$[t_3 \rightarrow t_4]$ Q_{1H} and Q_{2L} turns off, and the transformer current is now positive.

The steady state voltage transfer function is given by

$$\frac{V_{DC}}{V_{FC}} = \frac{n}{1-D}, \tag{1.18}$$

where D is the duty cycle, see Fig. (1.22) for the definition of D, and n is the transformer turns ratio. The current through the input inductor L_{FC} is given by Eq.æs (1.19) and (1.20) for charging and discharging respectively.

$$\Delta i_{L_{FC,charging}} = \frac{V_{FC} \cdot D \cdot T_S}{2 \cdot L_{FC}} \tag{1.19}$$

$$\Delta i_{L_{FC,discharging}} = \frac{(n \cdot V_{FC} - V_{DC}) \cdot (1-D) \cdot T_S}{2 \cdot L_{FC} \cdot n} \tag{1.20}$$

For steady state operation, Eq.æs (1.19) and (1.20) are equal to each other, except of their sign. Eq. 1.18 may easily be obtained by summing (1.19) and (1.20) and letting the resulting equation be equal to zero. The input voltage ripple is determined by the size of the input capacitor C_{FC} and the amount of ripple in the inductor current together with the switching frequency.

$$\Delta v_{FC} = \frac{\Delta i_{L_{FC}} \cdot T_S}{16 \cdot C_{FC}} \tag{1.21}$$

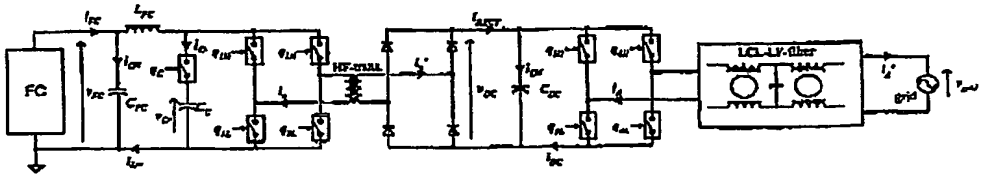


Figure 1.24: The *Active Clamped Current Source - Voltage Source Topology.*

Ratings

The voltage spike across the switches may be determined in terms of their output capacitances C_{oss} and the leakage inductance. The spike amplitude may be decomposed into two terms, one from the reflecting dc-link voltage, and the other from the leakage. The current delivered by the leakage inductance is poorly damped, and reaches a peak value of 2 times the FC inductor current. The peak voltage is then given by

$$\hat{V}_q = \frac{V_{dc}}{n} + \hat{i}_{L_{FC}} \cdot \sqrt{\frac{L_{lk}}{C_{oss}}} \tag{1.22}$$

The rms switch current is given by

$$I_q = \frac{I_{L_{FC}}}{2} \cdot \sqrt{2 - D} \tag{1.23}$$

for the leakage missing circuit, and approximated for the leakage included topology. The peak current is given above to approximate

$$\hat{I}_q = 2I_{L_{FC}} \tag{1.24}$$

In order to reduce the turn-off voltage spikes over the switches, it is necessary to reduce the transformer leakage inductance. If this not is possible, a snubber circuit must be added in parallel with the dc-link. A passive lossy snubber may be added, which will reduce the overall efficiency. Instead, one should use an active clamp circuit, as the one presented in the next section.

1.4.6 Active Clamped Current Source - Voltage Source

The Active Clamped Current Source - Voltage Source converter is depicted in Fig. 1.24, and the key waveforms in Fig. 1.25. The converter is based on a not so proven technology, and may therefore be less reliable then the solution presented in the previous sections. However, the added circuits seems not to be very complex, and it is therefore ours opinion, that the active clamp may be a good compromise between complexity, reliability and efficiency. The advantage for this topology is that the passive snubber is replaced with an active one, which

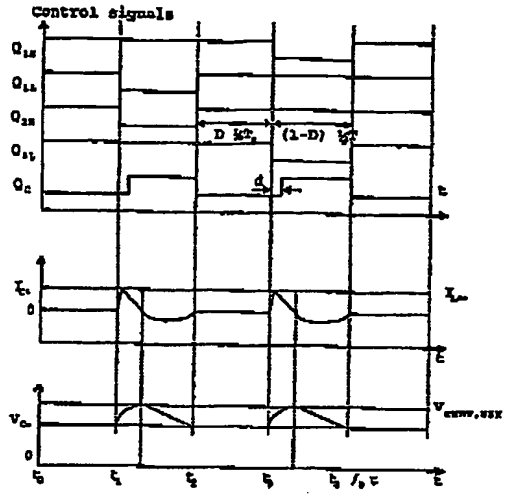


Figure 1.25: *Active Clamp CS-VS Converter waveforms.*

increases the overall efficiency, when compared with the CS-VS converter. The active clamp is switching on during zero current, and therefore only turn off losses may appear together with the forward voltage drop of the switch.

Mode of Operation

$[t_0 \rightarrow t_1]$ As in the CS-VS converter.

$[t_1 \rightarrow t_2]$ When transistors Q_{1L} and Q_{2H} turns off, the leakage current is discharged into the clamp capacitor C_C through the internal body diode of the clamp switch Q_C. This causes the voltage across the switches to raise slowly. The clamp switch Q_C is then turned on before the clamp current becomes negative, and zero current switching is in this way achieved. The capacitor current is now negative, causing the voltage to drop toward the reflected voltage from the dc-link.

$[t_2 \rightarrow t_3]$ As in the CS-VS converter.

$[t_3 \rightarrow t_4]$ Q_{1H} and Q_{2L} turns off.

The ripple current in L_{FC} and the ripple voltage across C_{FC} is equal to the ones given for the CS-VS converter.

ratings

The voltage spike across the switches is now given by

$$\hat{V}_q = \frac{V_{dc}}{n} + \hat{i}_{L_{FC}} \cdot \frac{\sqrt{4 \cdot L_{lk}}}{C_C} \tag{1.25}$$

for $C_C \gg C_{oss}$. The rms switch current is slightly lesser than

$$I_q = \frac{I_{L_{FC}}}{2} \cdot \sqrt{2 - D} \tag{1.26}$$

The peak current is given to

$$I_{L_{FC}} \leq \hat{I}_q \leq 2I_{L_{FC}} \tag{1.27}$$

The given expressions 1.26 and 1.27 are now very precise. However, the transistor supposed to be used in this application have current ratings in the area 82 A to 200 A @ 25° C.

1.4.7 Results

The CS-VS converter, with and without the active clamp, is designed according to the specifications given below:

Parameter	Value
V_{DC}	350 V
$V_{FC,noload}$	55 V
$V_{FC,nominalload}$	30 V
$\Delta V_{FC,nominalload}$	5 V
$\hat{V}_{q,secondary}$	55 V
$\hat{V}_{q,leakage}$	5 V
$I_{L_{FC}}$	20 A
$\Delta I_{L_{FC}}$	15 % $I_{L_{FC}}$
L_{lk}	0.3 μH
f_S	20 kHz

The minimum turns ratio is then given as $n = V_{dc}/\hat{V}_{q,secondary} \approx 7$. This yields a nominal duty cycle of 0.4, according to (1.18). For a maximum current ripple, of 3 A, in the input inductor together with the specifications in table 1.4.7 and (1.19), an inductor of 0.1 mH is reached. The input capacitor is designed by (1.21) to 1.9 μF. At last, the clamp capacitor is evaluated through (1.25) to 5.5 μF.
The following results is obtained by a simulation in PSIM. $r_{ds(on)} = 4.5\ m\Omega$ for Q_x and 30 $m\Omega$ for Q_c.

Parameter	CS-VS	Active clamped
$< V_{FC} >$	30.3 V	30.1 V
ΔV_{FC}	2.8 V	2.8 V
$\hat{V}_{qx}$	355 V	54.8 V
$< V_{dc} >$	348 V	348
I_{qx}	13.2 A	14.2 A
I_{qc}	-	9.4 A
$< I_{LFC} >$	19.8 A	19.9 A
ΔI_{LFC}	3.1 A	3.1 A
I_{trafo}	16.0 A	18.1 A
P_{in}	598.1 W	598.8W
P_{out}	594.0 W	592.1W
η	99.3	98.9

The three parameter with the largest deviation are the peak voltage across the switches, their current and the transformer current. The voltage spike across the switches is reduced from 355 V to 55 V, which is considered as being good. However, the rms current through the switches is raised with 1 A from 13.2 A to 14.2 A. That is because the transformer leakage inductance and the clamp capacitor forms a resonant tank, with a natural frequency of $\frac{1}{\sqrt{L_{lk} \cdot C_C}} = 123.9$ kHz (simulated to 125 kHz). This is also the reason why the transformer current is larger for the active clamped version.

1.5 Conclusion and selection of converter topology

Based on estimated losses in magnetics (conduction and iron), switches (conducting and switching) and diodes (conducting), the Current Fed Push Pull w/ Full Bridge Rectifier Converter seems to be the most promising topology for the dc/dc converter. The advantages for this converter are:

- Smooth input current
- Only two switches, also easy gate driver topology because both gates are referred to the same ground.
- Small ratio between Npri and Nsec.
- Possibility of adding more converters in parallel, without changing anything in the set-up or controllers

For the grid connected dc/ac inverter, the ordinary Full Bridge Inverter is chosen in the light of its advantages:

- No need for a transformer, like the push pull.

- Low dc-link voltage compared with the half bridge converter
- Presumably longer life time compared with the half bridge converter, because of the split dc-link capacitors.

In order to speed up the developing time, it have been chosen to use a modified Danfoss VLT 5001 frequency converter for the grid connected inverter.

35

Chapter 2

Design of the Current-Fed Push-Pull Converter

THE MAIN task is to design the converter with a minimum amount of loss and a minimum amount materials. These two opposite goals means that there is a trade off between the amount of used material and the obtained efficiency. This chapter describes the design which has been carried out for the selected current fed push pull converter. The passive elements are designed and a simulation model which includes losses is designed in order to analyse the converter load characteristic. The essential elements to be designed are:

Inductor: The input inductor of the current fed PP converter.

High-frequency Transformer: The push pull transformer.

Capacitors: Input capacitors to filter the inductor current.

SMPS: The internal switch mode power supply which delivers power to the control circuits.

Line filter: The grid connected LCL filter.

Designing the converter will be restricted by the following two limitations

- Thermally, the converter will be designed to the nominal power level operating point: V_{FC}=30 V, I_{FC}=20 A, P_{FC}=600 W.
- Electrically, the converter must be able to handle the peak power without bringing the transformer or the inductor into heavy saturation: V_{FC}=20 V, I_{FC}=46 A, P_{FC}=1150 W.

Table 2.1 shows characteristic values for the GPI at the four specified operating points. The design equations regarding magnetic design are listed in App. A.

P [W]	R [Ω]	V_{FC} [V]	$\frac{V_{DC}}{V_{FC}}$	D_L	D_q
60	2344.0	53.6	6.996	0.2139	0.6069
300	468.8	47.0	7.979	0.3107	0.6554
600	234.4	30.0	12.500	0.5600	0.7800
1150	122.3	25.0	15.000	0.6333	0.8167

Table 2.1: *Characteristic values at the four operating points.* $V_{DC} = 375$ *V,* $n = 5.5$.

2.1 Circuit waveforms

Fig. 2.1 shows schematic waveforms of the current fed push pull converter and fig. 2.2 shows simulated transformer voltages and currents at 600W with a transformer ratio at 5.5. Definition of time instances t_1 and t_2:

$$t_1 = D_L T_L = t_{on} = T_q(D_q - \frac{1}{2}) \tag{2.1}$$

$$t_2 = T_L = \frac{T_q}{2} \tag{2.2}$$

2.2 Electrical relations

This section provides the electrical relations used in the design.
The steady state transfer function is

$$\frac{V_{DC}}{V_{FC}} = n \cdot \frac{1}{1-D} = \frac{n}{Q} \tag{2.3}$$

where the transformer ratio is given by

$$n = \frac{N_s}{N_p} \tag{2.4}$$

and $D + Q = 1$.

$$T_L D_L = T_q(D_q - \frac{1}{2}) \quad \wedge \quad T_q = 2T_L$$

$$D_L = 2D_q - 1 \quad \text{or} \quad D_q = \frac{D_L + 1}{2} \tag{2.5}$$

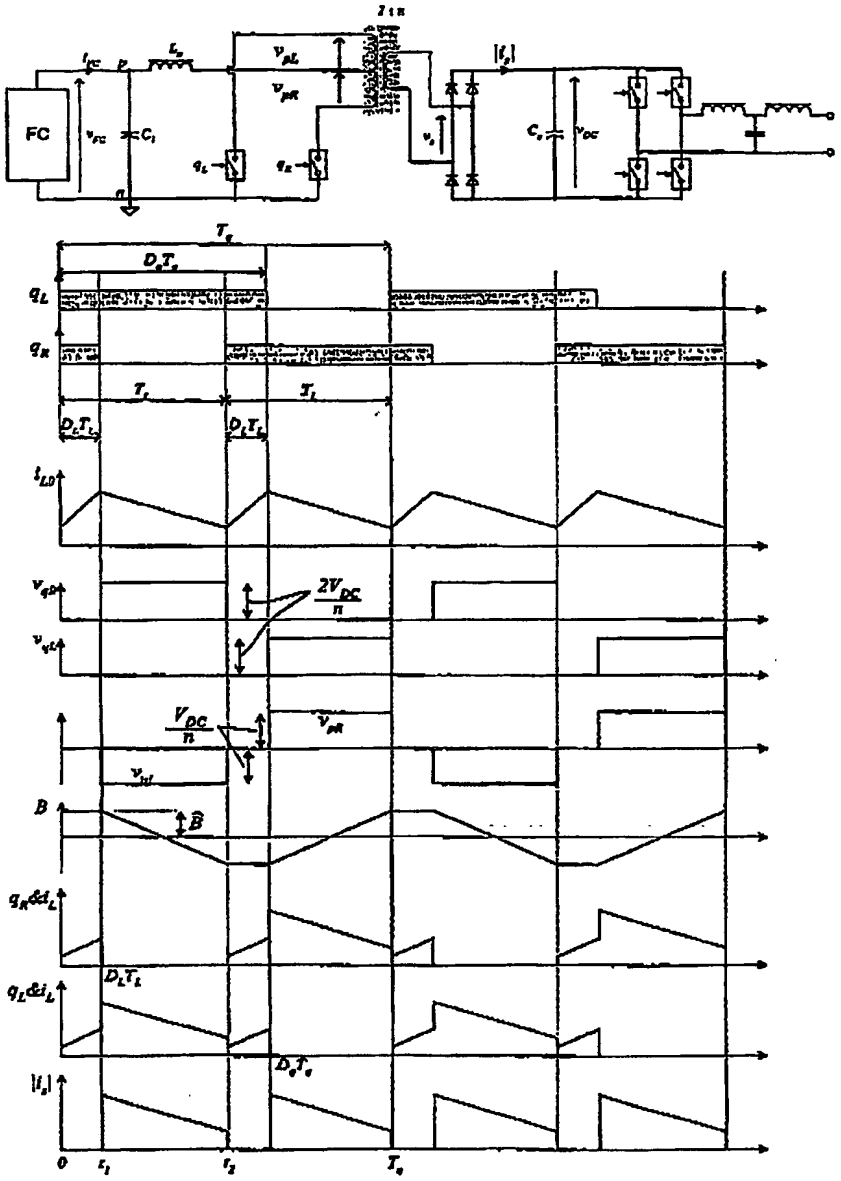


Figure 2.1: *Waveforms of the current fed push pull converter.*

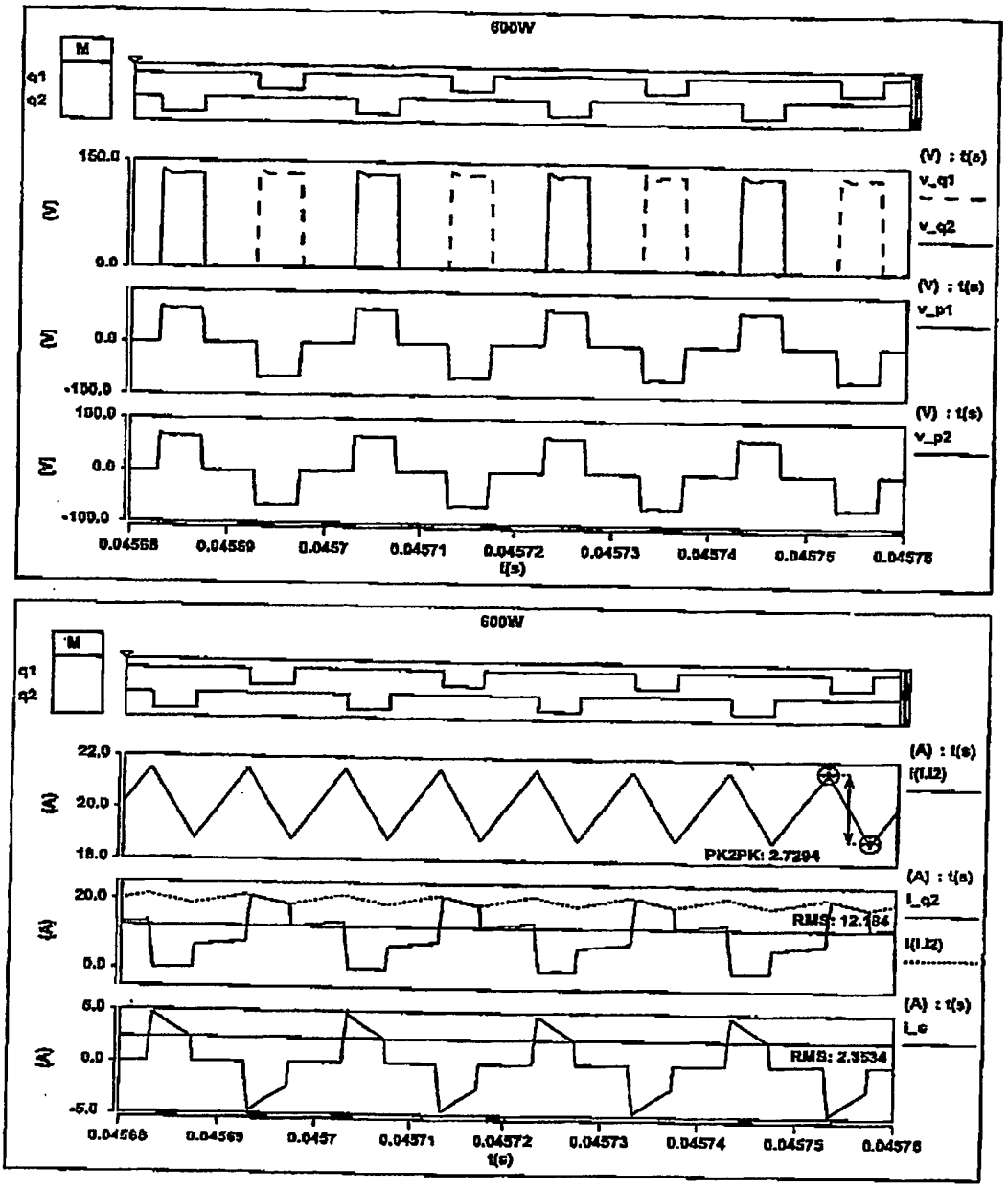


Figure 2.2: *Transformer voltages and currents at 600W.* $n_{trafo} = 5.5$.

Thus

$$n_{min} = 15(1 - D_L) \tag{2.6}$$
$$= 30(1 - D_q) \tag{2.7}$$

$$D_L = 1 - n \cdot \frac{V_{FC}}{V_{DC}} \quad \Leftrightarrow \quad n = \frac{V_{DC}}{V_{FC}} \cdot (1 - D_L) \tag{2.8}$$
$$D_q = 1 - \frac{n}{2} \cdot \frac{V_{FC}}{V_{DC}} \quad \Leftrightarrow \quad n = 2 \cdot \frac{V_{DC}}{V_{FC}} \cdot (1 - D_q) \tag{2.9}$$

$$\hat{v}_{prim} = \frac{\hat{V}_{DC}}{n} \tag{2.10}$$
$$\hat{v}_{switch} = 2 \cdot \hat{v}_{prim} = 2 \cdot \frac{\hat{V}_{DC}}{n} \tag{2.11}$$

Time description of the inductor current (cf. fig. 2.1):

$$i_L(t) = \begin{cases} i_L(0) + \frac{V_{DC}}{L} \cdot t & \text{for } t\text{: } 0 \rightarrow t_1, \\ i_L(t_1) + \frac{nV_{FC} - V_{DC}}{nL} \cdot (t - t_1) & \text{for } t\text{: } t_1 \rightarrow t_2. \end{cases} \tag{2.12}$$

2.2.1 RMS and average values

This section describes the rms-values of different currents in the circuit , cf. fig. 2.1.
The inductor current:

$$\mathbf{t : 0 \mapsto t_1}$$
$$i_L = \check{i}_L + \frac{\Delta i_L}{t_1} \cdot t$$
$$\mathbf{t : t_1 \mapsto t_2}$$
$$i_L = \hat{i}_L - \frac{\Delta i}{t_2 - t_1} \cdot (t - t_1) = \frac{\Delta i}{t_1 - t_2}(t - t_1) + \hat{i}_L$$

The square of the inductor current:

$$\mathbf{t : 0 \mapsto t_1}$$
$$i_L^2 = \left(\frac{\Delta i}{t_1}\right)^2 t^2 + \left(\frac{2\Delta i \cdot \check{i}_L}{t_1}\right) \cdot t + \check{i}_L^2$$
$$\mathbf{t : t_1 \mapsto t_2}$$
$$i_L^2 = \left(\frac{\Delta i}{t_1 - t_2}(t - t_1) + \hat{i}_L\right)^2$$
$$= \left(\frac{\Delta i}{t_1 - t_2}\right)^2 \cdot (t^2 - 2t_1 t + t_1^2) + \frac{2\Delta i \cdot \hat{i}_L}{t_1 - t_2} \cdot (t - t_1) + \hat{i}_L^2 \tag{2.13}$$

Integration of the square of the inductor current

$$
\begin{aligned}
&t: 0 \mapsto t_1 \\
&\int_0^{t_1} i_L^2 dt = \int_0^{t_1} \left[\left(\frac{\Delta i}{t_1} \right)^2 t^2 + \left(\frac{2\Delta i \cdot \check{i}_L}{t_1} \right) \cdot t + \check{i}_L^2 \right] dt \\
&\qquad = \left[\frac{(\Delta i)^2}{3} + \Delta i \cdot \check{i}_L + \check{i}_L^2 \right] t_1 \qquad (2.14) \\
&t: t_1 \mapsto t_2 \\
&\int_{t_1}^{t_2} i_L^2 dt = \int_{t_1}^{t_2} \left[\left(\frac{\Delta i}{t_1 - t_2} \right)^2 \cdot (t^2 - 2t_1 t + t_1^2) + \frac{2\Delta i \cdot \check{i}_L}{t_1 - t_2} \cdot (t - t_1) + \check{i}_L^2 \right] dt \\
&\qquad = \left(\frac{\Delta i}{t_1 - t_2} \right)^2 \cdot \left[\frac{t_2^3 - t_1^3}{3} - t_1(t_2^2 - t_1^2) + t_1^2(t_2 - t_1) \right] \\
&\qquad + \left(\frac{2\Delta i \cdot \check{i}_L}{t_1 - t_2} \right) \cdot \left[\frac{t_2^2 - t_1^2}{2} + t_1(t_1 - t_2) \right] + \check{i}_L^2 \cdot (t_2 - t_1) \qquad (2.15)
\end{aligned}
$$

The following rms currents can be calculated from the above listed equations:

$$I_L = \sqrt{\frac{1}{T_L} \left[\int_0^{t_1} i_L^2 dt + \int_{t_1}^{t_2} i_L^2 dt \right]} \qquad (2.16)$$

$$I_q = \sqrt{\frac{1}{T_q} \left[2 \cdot \int_0^{t_1} i_L^2 dt + \int_{t_1}^{t_2} i_L^2 dt \right]} \qquad (2.17)$$

Thus, the rms currents are nonlinear functions of the duty cycle and the current ripple: $I_x(\Delta i, t_1, t_2, T_q, T_L) = I_x(L, f_L, d_L)$.

2.3 Designing the converter

The converter losses may be distributed into four categories as in tab. 2.2 or mathematically

$$
\begin{aligned}
& P_{C_{FC}}(\Delta i_L, f_L) \\
& P_L(\Delta i_L, f_L, l_g, I_L, N_L, V) \\
& P_{sw}(\Delta i_L, f_q, I_q, T_{on}, T_{off}) \\
& P_{trafo}(\Delta i_L, f_q, I_{trafo}, n, N_p, V, \text{winding configuration}) \\
P_{total} &= P_{C_{FC}} + P_L + P_{MOS} + P_{trafo} \qquad (2.18)
\end{aligned}
$$

where $P_{C_{FC}}$ is the loss in the input capacitor, P_L are the losses in the inductor, P_{sw} are the losses in switches and diodes, and P_{trafo} is the losses in the transformer.

Parameter	Designation	Input Cap.	Boost ind.	Switches	Transformer
Current ripple	Δi_L	√	√	√	√
Inductor frequency	f_L	√	√		
Switch frequency	f_q			√	√
Air gap	l_g		√		
Switch rms current	I_q			√	√
Inductor rms current	I_L	√	√		
Inductor number of turns	n_L		√		
Trafo. number of turns	n		√		√
Turn off/on times	T_{off}/T_{on}			√	
Physical size /volume			√		√
Winding Layout			(√)		√

Table 2.2: *Parameters to specify the losses.*

Designing the converter for high efficiency all the above listed components must be included and their interaction. The inductor current ripple Δi_L and the frequency f_L ($f_L \propto f_q$) are two global parameters which are chosen for the analysis - the other parameters are treated as local parameters. Thus the design goal is to solve the following equation

$$\text{Design goal: } \min_{f_L,\ \Delta i_L} P_{total} = \min_{f_L,\ \Delta i_L} (P_{Crc} + P_L + P_{MOS} + P_{trafo}) \tag{2.19}$$

The losses for each part have been derived. The design gave the following general parameter:

-a switching frequency at 35kHz!

In the next sections the losses for these four parts will be shown.

2.4 Design of transformer

The transformer is in many ways the key element in the dcdc converter and therefore it cannot not be designed separately. Many tradeoffs have been evaluated during the design of the transformer. This has been an iterative process because almost each design was reralised, tested and evaluated. The design follows the description in App. A and the transformer was tested in the push pull circuit. The main problems in the design:

- To lower the magnetic loss by decreasing the peak induction by increasing the number of turns and still having enough space for the conductors.
- To minimize the leakage inductance between the two primary windings as a high coupling is required in order to have a high efficiency.

Parameter	Value
V_{DSS}	200 V
$I_{D,25°C}$	83 A
$R_{DS(on)}$	25 $m\Omega$
$V_{GS(th)}$	2...4 V
C_{iss} ($V_{DS} > 5$ V)	9nF
$g_m(I_D)$	$6.3 \cdot I_D$ $^{0.6}$

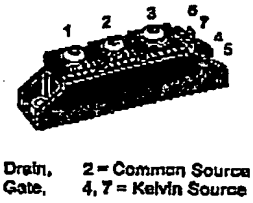


Figure 2.3: *The MOSFET VMK 90-02T2. The most important data and a drawing.*

- To limit the volume of the transformer.

In order to have a high coupling between the two primary windings different approaches was tested: Litz wire and foil wire was tested and it was found that the best coupling and the best utilization of the available space for windings was achieved when using foil wire as primary winding. Also for these wire-types different core types and sizes was tested. It was found that the ETD core 59 (the biggest ETD core) has to little space for the windings - if the efficiency target should be reached at 35kHz. Instead a EE70/32.7 was used successfully. The parameters for the final transformer is

- 7 primary turns per winding.
- a 0.15x38mm foil is used for the primary.
- The two primary windings is wound bifilar.
- 2x25 secondary turns each consisting of 3x0.7mm ordinary round wire. Thus, a total of 50 turn secondary giving a turns ration close to 7.
- The transformer core is EE70/32.7 and the material is N67.
- The two primary windings are placed in the middle and each half of the secondary is placed on each side.

2.5 Switches and Gate drive

2.5.1 MOSFETS

The MOSFET VMK 90-02T2 is selected, after a study of available switches. It is selected due to its relative low on resistance. Other MOSFETs may be used later on.

2.5.2 Gate Drive

The gate drive circuit is depicted in Fig 2.4. The drivers is designed with respect to switching losses and over-voltages due to the transformer leakage inductance.

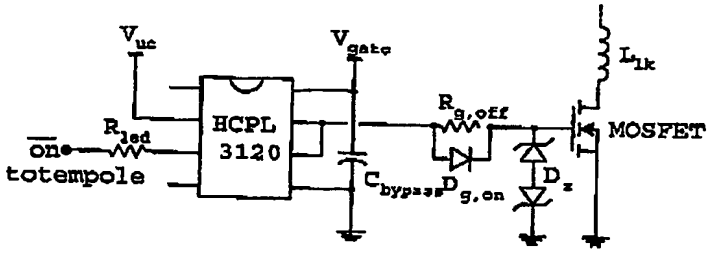


Figure 2.4: *Gate drive circuit. A 0.1 μF bypass capacitor must be connected between pins 5 and 8.*

Design and Layout

The gate drivers are realized with the HCPL-3120 IC. This circuit supports galvanic isolation between the command signal, and the MOSFET. Moreover, is it capable of driving a 2.0 A current through the gate of the MOSFET. The most important data are given in figure 2.5.
To keep the MOSFET firmly off, the HCPL-3120 has a very low maximum V_{OL} specification of 0.5 V. The HCPL-3120 realizes this very low V_{OL} by using a DMOS transistor with 1 Ω (typical) on resistance in its pull down circuit. When the HCPL-3120 is in the low state, the MOSFET gate is shorted to the source by $R_{g,off} + 1\Omega$.
The off resistance is after some trial and error found to 3Ω. The power loss in the clamp and the MOSFET depends on the off resistance. Low off resistance ⇒ low MOSFET loss and high clamp loss. High off resistance ⇒ high MOSFET loss and low clamp loss.

Parameter	Value
V_{cc}	15 ... 30 V
$I_{F(on)}$	10 ... 16 mA
$V_{F(off)}$	−3.0 ... 0.8 V
I_{OH}	2.0 A
I_{OL}	2.0 A

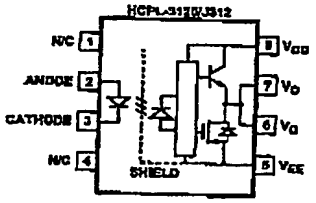


Figure 2.5: *The 2.0 Amp Output Current MOSFET Gate Drive Optocoupler HCPL-3120. The most important data and a drawing.*

The selection of the on resistance is less critical, while the other MOSFET carries (almost) the entire current while it turn on, so no additional losses appears.
The current limiting resistor R_{led}, in the LED driving circuit, is given to 270 Ω from Agilent Technologies.
A gate-source snubber circuit may be added, in order to damp any possibly ringing in the gate-source voltage. It may be formed by a RC circuit in parallel with the gate-source, or a ferrite bead on the gate.

2.6 Input Filter

The input filter is depicted in Fig. 2.6. The input filter is made up of the capacitor C_{FC} and the inductor L_{FC}. The fuel cell is replaced with itæs Thvenin equivalent circuit, that are $V_{FC,noload}$ and R_{FC}. The push-pull converter is replaced with a boost converter, with a switching frequency equal to twice the frequency of the push-pull converter.

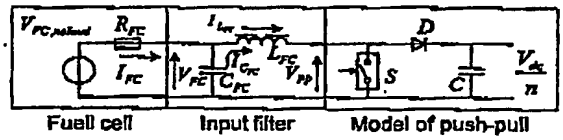


Figure 2.6: *The input filter, together with the fuel cell and a model of the push-pull converter.*

The input filter will be designed, so that the specifications for the fuel-cell ⇔ converter interface are respected. Moreover, the wire- and core-losses in the inductor is the design parameters that has to be optimized, in term ripple in the inductor current.

2.6.1 Circuit Modeling

The steady state voltage gain is given by:

$$\frac{\langle V_{dc}\rangle}{\langle V_{FC}\rangle \cdot n} = \frac{1}{1-D} \tag{2.20}$$

where D is the duty cycle and n is the transformer turns ratio. The steady state average current through L_{FC} is given by

$$\langle I_{L_{FC}}\rangle = \frac{V_{FC,noload} - \langle V_{FC}\rangle}{R_{FC}} = \frac{n \cdot V_{FC,noload} - \langle V_{do}\rangle(1-D)}{n \cdot R_{FC}} \tag{2.21}$$

The current ripple (peak-peak) is given by

$$\Delta I_{L_{FC}} = \frac{\langle V_{FC}\rangle D \cdot T_S}{2L_{FC}} = \frac{\langle V_{dc}\rangle (1-D) D \cdot T_S}{2nL_{FC}} \tag{2.22}$$

The instantaneous inductor current is given by

$$i_{L_{FC}} = \langle I_{FC}\rangle + \Delta I_{L_{FC}} \cdot \begin{cases} \left(\frac{2t}{T_S D} - \frac{1}{2}\right) \text{ for } 0 \le t \le \frac{DT_S}{2} \\ \left(\frac{T_S D - 2t}{T_S(1-D)} + \frac{1}{2}\right) \text{ for } \frac{DT_S}{2} \le t \le \frac{T_S}{2} \end{cases} \tag{2.23}$$

and the rms value as

$$I_{L_{FC}} = \langle I_{L_{FC}}\rangle \sqrt{1 + \frac{1}{12}\left(\frac{\Delta I_{L_{FC}}}{\langle I_{L_{FC}}\rangle}\right)^2} \tag{2.24}$$

The instantaneous FC current is given by

$$i_{FC} = \frac{V_{FC,noload} - v_{FC}}{R_{FC}} \tag{2.25}$$

and the instantaneous capacitor current is given by

$$i_{C_{FC}} = i_{FC} - i_{L_{FC}} \tag{2.26}$$

At last, the voltage over the fuel cell is given by

$$v_{FC} = \frac{1}{C_{Fc}} \int i_{FC} - i_{L_{FC}}\, dt \tag{2.27}$$

Equations (2.23) to (2.27) describes the filter circuit by means of a linear differential equation. This equation may be written as

$$y' + p(t) \cdot y = r(t) \tag{2.28}$$

where

$$y' = v_{C_{FC}}', \; y = v_{C_{FC}}, \; p(t) = \frac{1}{R_{FC}C_{FC}} \text{ and } r(t) = -\frac{i_{L_{FC}}}{C_{FC}} \tag{2.29}$$

The nonhomogeneous equation (2.28) is solved, with respect to y. The solution is given in [Kreyszig] as

$$y(t) = e^{-h} \cdot \left[\int e^{h} \cdot r(t)\, dt + c \right], \; h = \int p(t) dt \tag{2.30}$$

The LDE given in (2.28) is solved numerical in the developed MATLAB programme, and the peak peak voltage is given by searching the data.

2.6.2 Filter Capacitor

The overall design goals for the filter capacitor in this section are:

- Obtain a specified capacitance.
- Evaluate the power loss, in order to determine the temperature raising.
- Evaluate the maximum $\frac{dv}{dt}$.

The first item is easy to keep. The voltage class is directly given by the fuel cells noload voltage. The size of the capacitor is found from (2.30) together with the specification for the maximum allowable voltage ripple. Excessive rms current will cause the capacitor to overheat. The power loss in the capacitor is given as

$$P_{cap} = \sum_{n=1}^{N} I_{C_{FC},n}{}^2 \cdot ESR_n \tag{2.31}$$

The capacitor ESR is given in the Evox-Rifa programme æPulse Capacitor CAD V 1.2æ, and the n^{th} capacitor current is found through a simulation. The losses causes the internal temperature of the capacitor to rise. The internal temperature is given by

$$T_h = P_{cap} \cdot R_{\theta,ha} + T_a \tag{2.32}$$

where T_h is the hot spot temperature, $R_{\theta,ha}$ is the thermal resistance between hot spot and ambient, and T_a is the ambient temperature. Excessive instantaneous current can destroy the capacitor leads and the attachments to the leads. The instantaneous current is stated in terms of the rate of voltage change, $\frac{dv}{dt}$. Assuming that the entire ripple current is bypassed by the capacitor, the rate of change is given by

$$\frac{dv}{dt} = \frac{\Delta I_{L_{FC}}}{2C_{FC}} \tag{2.33}$$

The rate given above must not exceed the value given in the data sheet.

2.6.3 Design of Input Inductor and Capacitor

The equations given in the previous section and appendix A, are now used to find an optimized inductor and capacitor. The following specifications are used

Inductor

In order to raise the efficiency, it is decided to use the Siemens N87 ferrite, for the core. The saturation flux density for the N87 material is given in table 2.5. The other material constants are give in table 2.4. All parameters are deduced from the data sheet.

2.7 Switch Mode Power Supply

2.7.1 Specs

The supply for the GPI will be based on the fly back topology, while the GPI consumes only approximate 9.5 W. The approximate power levels for the various circuits is given below.

Name	No. in Fig 2.10	Voltage [V]	Power [W]
Push-pull control and microprocessor	1	+15 V, +7.5 V, -15 V	4.0 W, 1.3 W, 1.6 W
Mains side measurements	3	+5 V	0.6 W
Push-pull gate drive	4	+15 V, -15 V	1.3 W, 0.3 W
DC-link measurement, inrush and self supply	2	+17.5 V, +7.5 V	1.6 W, 0.5 W

Table 2.8: *The voltage and power levels for the supplies. The power levels are based on data sheets and measurements.*

Moreover, the allowable voltage ripple (ΔV_{out}) due to the switching, is set to 2 mV. It becomes then possible to determine the size of the output capacitors. The input voltage to the supply is takes from the dc-link of the VLT. In this way, it is assured that there always is power available, even though if the mains or the fuel cell voltages falls out. The input voltage (V_{in}) is then given to 350 V. The nominal duty cycle (D) is selected to 0.2. The switching frequency (f_s) is selected to 50 kHz. The efficiency (η) is first set to 0.7. which approximates to an input power (P_{in}) equal to 14.3 W.

2.7.2 Analysis

The needed permeability is given by (2.37)

$$\mu_{r,needed} = \frac{B_{sat}^2 \cdot l_e \cdot A_e \cdot f_s}{2 \cdot P_{in} \cdot \mu_0}, \tag{2.37}$$

where B_{sat} is the saturation flux density, l_e is the magnetic mean length and A_e is the magnetic cross area. The minimum airgab is then given by (2.38)

$$l_{g,min} = \frac{l_e \cdot (\mu_r - \mu_{r,needed})}{\mu_r \cdot \mu_{r,needed}}, \tag{2.38}$$

where μ_r is the initial permeability. On the other hand, the airgab may not be to small, because the transformer then becomes inductance dead. This means that the current cannot reach the required value in $D_{nom} \cdot T_s$ seconds. The maximum allowable inductance is given by (2.39)

$$L_{max} = \frac{V_{in}^2 \cdot D^2}{2 \cdot P_{in} \cdot f_s}. \tag{2.39}$$

The minimum airgab is then given in (2.40)

$$l_{g,Lmax} = \frac{N_p^2 \cdot \mu_0 \cdot \mu_r \cdot Ae - L_{max} \cdot l_e}{L_{max} \cdot \mu_r}, \tag{2.40}$$

where N_p is the primary number of turns. The turns ratio between the primary and the secondary windings is given by (2.41)

$$n_n = \frac{N_{s,n}}{N_p} < \frac{V_{out,n} \cdot (1-D)}{V_{in} \cdot D}, \tag{2.41}$$

where $N_{s,n}$ is the secondary number of turns of the n^{th} winding. The minimum required number of primary turns can be found by (2.42)

$$N_{p,min} = \frac{V_{in} \cdot D}{B_{sat} \cdot A_e \cdot f_s}. \tag{2.42}$$

At last, the skin depth is given by (2.43)

$$\delta = \frac{66.1}{\sqrt{f_s}}[mm]. \tag{2.43}$$

The allocated space for each winding, is given by (2.44)

$$\alpha_n = \frac{N_n \cdot I_n}{\sum N \cdot I}, \tag{2.44}$$

where the sum is the total turns-ampere and N_n and I_n is the respectively number of turns and rms current for the n^{th} winding. The rms current is given by $\hat{i} \cdot \sqrt{D/3}$. For the primary side, D is equal to the nominal duty cycle, whereas for the primary windings it is equal to $d = D \cdot N_{s,n}/N_p \cdot V_{in}/V_{out,n}$. This is because the charge- and discharge-times of the transformer is not equal. The peak value is given by $\hat{i}_n = 2 \cdot P_{out,n}/(V_{out,n} \cdot d)$. The number of stands in the Litz-wire is then given by (2.45)

$$\#_{wire,n} = floor\left(\frac{A_N \cdot \alpha_n \cdot K_u}{N_n \cdot A_{wire}}\right), \tag{2.45}$$

where $\#_{wire,n}$ is the number of wires in the Litz, A_N is the window area, K_u is the window fill factor (K_u=0.4) and A_{wire} is the area of each strands. The size of the output capacitors is given by (2.46)

$$C_n = \frac{\hat{i} \cdot d \cdot (2-d)^2}{2 \cdot \Delta V_{out} \cdot f_s}, \tag{2.46}$$

Design

The transformer is now to be designed. As a starting point, the core is selected to be the ETD44 made of the material 3C90. The following data is provided by Philips.

B_{sat} @ 50 kHz	300 mT
l_e	78.6 mm
A_e	97.1 mm^2
μ_r @ 100 °C	3700
A_N	123 mm^2

Table 2.9: *Constant for the ETD44 core made of 3C90.*

By using (2.37) to (2.46) together with the specifications and the data given in table 2.9 the following results are obtained:

No. in Fig 2.10 and Voltage	Number of turns N	Number of strands in Litz $\#$	Output capacitance [μF]
Primary	55	1	-
1, +15 V	9	6	1100
1, +5 V	3	5	500
1, -15 V	9	2	400
2, +15 V	9	2	400
2, +5 V	3	2	300
3, +5 V	3	2	300
4, +15 V	9	2	300
4, -15 V	9	1	300

Table 2.10: *Output from computations for the trafo. The length of the airgab is computed to 0.062 mm. The maximum allowable inductance is computer to 3.5 mH, and an airgab of minimum 0.084 mm must be applied, the transformer will otherwise be inductance-dead. The used wire have a diameter of 0.4 mm.*

2.7.3 Test

The GPI-SMPS is tested in order to reveal that the design is OK. The output voltage is adjusted, until a reasonable value is found. The values are given in table 2.11.

Voltage	Micro 15.05 V	Micro -14.94 V	Micro 5.00 V	Mains 5.24 V	DC-link 8.75 V	FC 15.32 V	FC -16.45 V
Load resistance	57.1 Ω	140.5 Ω	29.0 Ω	70.0 Ω	66.7 Ω	181.0 Ω	750 Ω
Power	3.96 W	1.59 W	1.28 W	0.57 W	0.48 W	1.30 W	0.32

Table 2.11: *The total output power equals 9.5 W. The input power, evaluated over 1 hour, is 14.1 W. The efficiency is then 0.67. The measurements are made after a 25h26m burn-in test.*

2.7. Switch Mode Power Supply

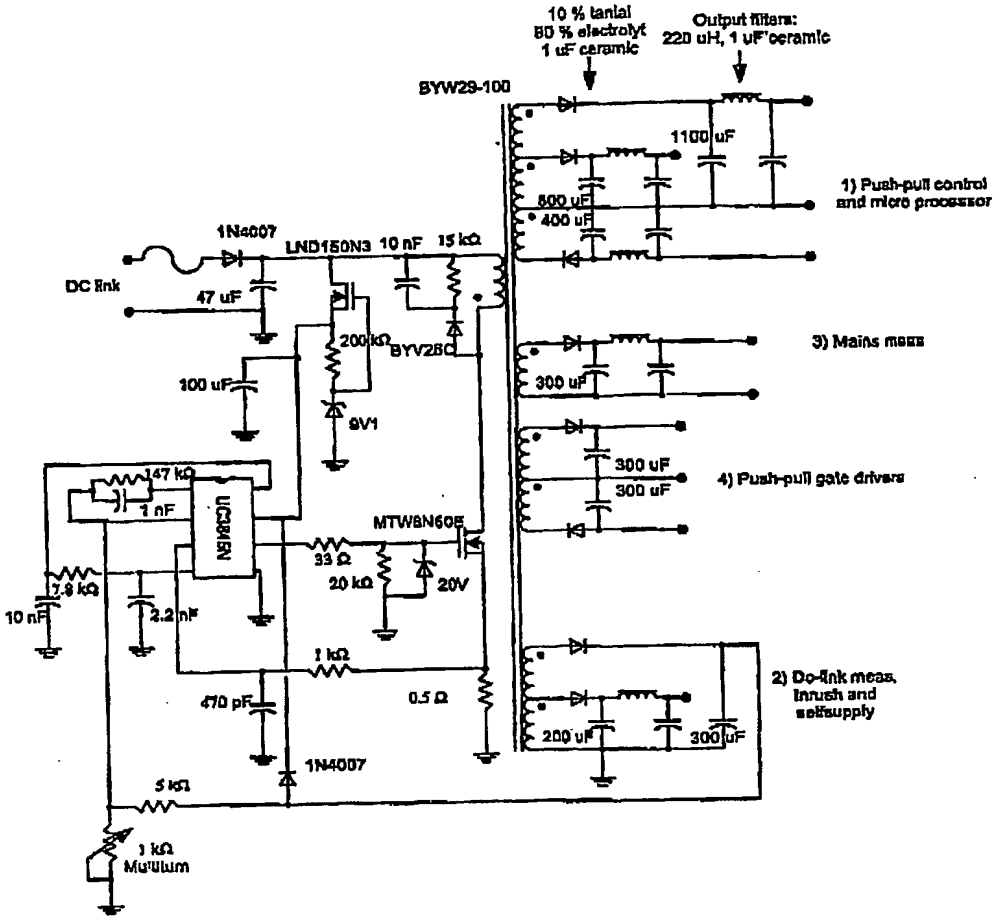


Figure 2.10: *The schematics for the GPI-SMPS. Five of the outlets have additional filters. The values for the components are:* $L_{filter} = 220\mu H$ *and* $C_{filter} = 1\mu F$*. The natural frequency is then approximate 11 kHz.*

2.8 Design of Output Filter

The inductors used for the voltage to current transformation is now designed. Two inductors are made, one for each phase. The phases becomes in this way ground fault protected, while the current cannot raise infinite fast. The hardware protection then have time to react and turn off the IGBTs. The specifications for the inductors are given in table 2.12

Inductance L	2 * 2.15 mH
Maximum current	$\frac{1000W \cdot 0.88}{230V \cdot 0.9} \sqrt{(2)} = 6.0$ A

Table 2.12: *Specs for the VLT inductors.*

The inductors are designed according to appendix A. The core for the inductors are selected to the ETD54 grade 3C90 from Philips. The minimum air gab is computed to 3 mm, which correspond to 137 turn. With 137 turns, there is space for a wire diameter equal to 1.4 mm.
The inductor was made and tested. The total inductance is measured to 4.2 mH @ (50 Hz & 6 A). The total resistance (both copper and equivalent iron resistance) was in the same test measured to 0.33 Ω.

2.9 Summary

The current fed push pull converter is designed in order to minimize the losses.The losses of all the elements have been taking into account and the total minimum amount of loss was the design criteria. Also the desing of the internal power supply is shown. The next two chapters will treat the implementation and testing of the designed converter.

57

Chapter 3

Implementation issues of the Current-Fed Push Pull Converter

AS IT has been shown before, the control of the Push Pull (PP) converter uses an analog PI controller to deliver a command signal to a dedicated dual PWM generator. In conjunction to this analog control, a logic control unit implemented in a Programmable Logic Device (PLD) is employed in order to provide the necessary protections and to improve the flexibility, as a controlled soft start-up of the converter in voltage mode, driven by the micro controller.

3.1 The controller for the Push-Pull Converter

The design of the PP-current controller (in conjunction with the application note). This controller has the following requirements:

- to accept reference signal from the microcontroller
- to include a PI controller for the inductor current
- to convert the output signal from the PI current controller in pulses for the PP transistors
- to include auxiliary circuits to provide soft start-up of the converter, antiwindup, and to provide galvanivaly insulated analog signals to the microcontroller of the FC voltage and current

Fig. 3.1 shows the control diagram of the PP.

3.2 PWM Modulator

It has been chosen a PWM modulator chip, designed for driving the two transistors in Push-Pull configuration. The span of the control voltage is given in the catalog 0-5V, but

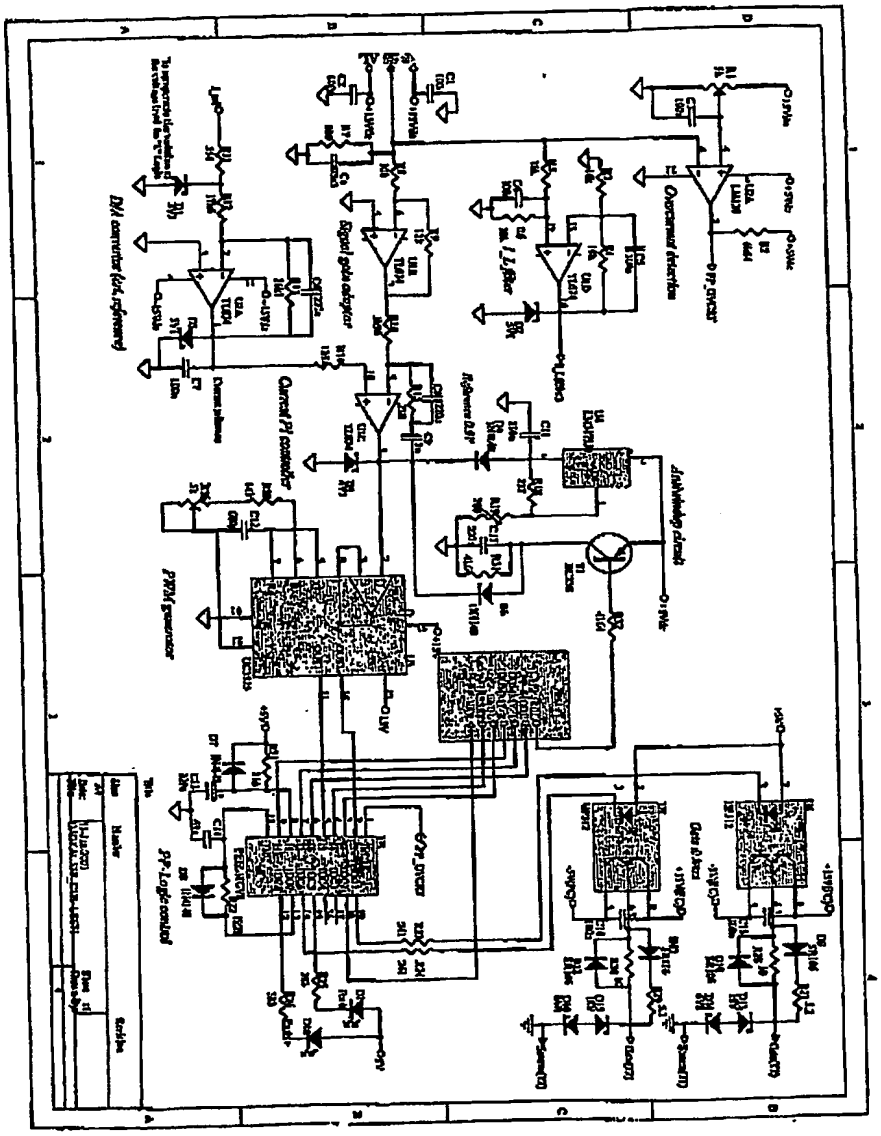


Figure 3.1: *Push Pull Control diagram.*

continuous variation of the duty-cycle is provided only between 0.9 V - 3.6V. From 3.3 V to 5V, the duty-cycle remains unchanged (about 47%), while below 0.9 V, the duty-cycle of the pulses changes suddenly from about 5% to zero (no pulses). This is shown in fig. 3.2.

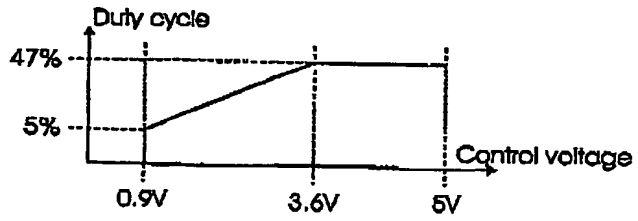


Figure 3.2: *Transfer characteristic of the SG3525 analog PWM generator.*

The circuit (SG3525) is designed to drive voltage mode Push Pull Converters, therefore, the command signals should be inverted before driving the gate-drivers. As a precaution, an anti-windup circuit was employed, to provide continuous operation of the PP, in any kind of conditions.

3.3 Soft startup of Push-Pull Converter

In order to avoid over currents during start-up, caused by the unmagnetized transformer or the saturation of the analog PI controller which may cause overshooting of the control-signal, auxiliary circuit should be used. These consist of:

- an anti-windup circuit (U4-D4-R18-R19-C11-D5), on both upper (4.7 V) and lower (0.9 V) limit of the PI controller output, which gives the possibility to have continuous pulse generation.
- a controllable minimum switch overlap duty-cycle circuit, which gives the possibility to force the Push-Pull converter to work with minimum switch overlap duty-cycle, meaning minimum power in DC-link, commanded from the microcontroller when needed;
- extra functional logic found in a PLD, to allow direct command of the PP transistors from the micro controller, when needed.
- few digital outputs from the microcontroller, controlled by software;

All these subcircuits form a hybrid regulator (analog& digital), able to react very fast (characteristic for analog control) in order to control the current in the inductor, and also,

providing flexibility (characteristic for digital control) in order to solve easily all the required tasks needed by a fully functional prototype.

In order to be able to start-up the Push-Pull converter without overcurrents, is necessary to ramp-up the duty-cycle in voltage mode, from zero duty-cycle to 50% and beyond, when this goes in current mode, until it reaches the minimum limit of the switch overlap duty-cycle given by the analog modulator. In this way, any shock is eliminated. However, due to the presence of the inductance in the circuit, during voltage mode much energy is produced, which flows into the clamp circuit. Therefore, this ramping should be completed fast, and it should be verified if the clamp circuit is able to withstand the transient without exceeding the safe operation voltage level.

Investigations to implement the previously announced start-up principle exclusively by analog circuitry gave no result, therefore it has been chosen to produce with the micro controller the two-desired controllable duty-cycle 180° shifted pulses, by using two digital outputs driven by the Capture-Compare Unit. To be able to control directly the gate driver by these signals, another signal to select the source (analog PW-Modulator or microcontroller) should be used. In Fig. 3.3, the principle of generation of the pulses is shown. Timer T0 is running continuously with a frequency very close to the analog PWM generator. Digital outputs P8 and P9 are programmed to work in mode 3, commanded by CC8 and CC9, which are both assigned to timer T0.

The pulses are not equally placed, because of software simplicity, but also, because is possible to reduce the energy which flows in the clamp circuit when a firing pulse is immediately following a previous firing pulse in the Push Pull converter. Also, it is easy to overlap the pulses, by making CC9 smaller than CC8, and performing smoothly the transition from voltage mode to current mode.

In order to eliminate overshoots of the analog control, when the converter is started, or when the command is switched back to the analog PW Modulator, a circuit to force the PI controller output, being controlled from the microcontroller by a digital output is necessary. This circuit (T1-D6-R31-C17) should force the output of the PI controller to be higher than 3.6V, which corresponds to the minimum switch overlap duty-cycle when commanded from microcontroller, and to ensure a smooth transition to steady state when command is released (R31-C17).

In Fig. 3.4 the evolution of the control signals during the start-up is shown. The converter starts driven by pulses produced by the microcontroller, with a variable duty-cycle, ramping to a value, which corresponds to the minimum switch overlapping duty-cycle, specific to the analog controller. Therefore, at the end of the ramping, the converter goes smoothly from voltage mode to current mode. All this time, the output of the PI controller

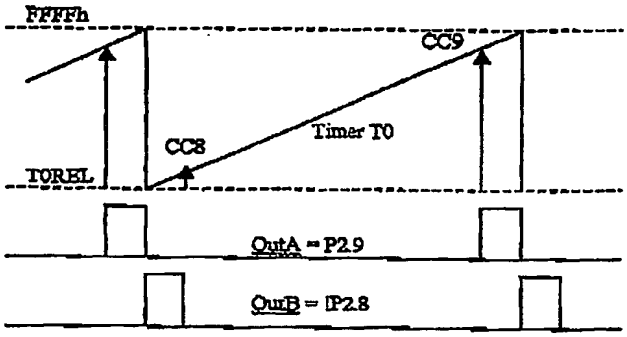


Figure 3.3: *Generation of pulses for operation in voltage mode.*

is clamped to a value, which applied to the PWM generator, produces the same duty-cycle synthesized by the microcontroller at the end of the ramp. Therefore, when the source of the pulses is switched from microcontroller to the analog PWM generator, no transient should appear. Only after the output of the PI controller is softly released, the duty-cycle of the switches may vary freely, in order to regulate the inductor current at the desired level.

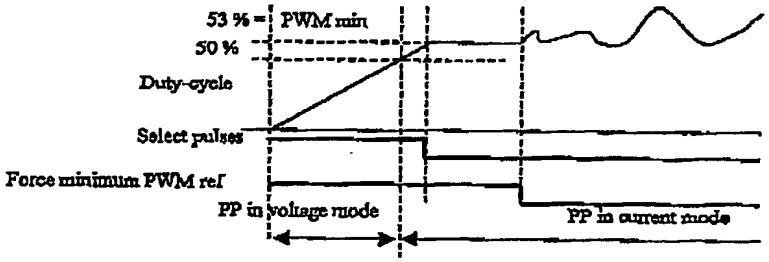


Figure 3.4: *Evolution of the control signals during PP startup.*

In Fig. 3.4 is illustrated the successful start-up of the PP converter.

3.4 D/A converter

This is used to interface the microcontroller with the analog control of the PP converter, in order to vary the reference current of the PP converter in respect to the FC characteristics. As the microcontroller has ho D/A port, it is necessary to convert a digital signal, which is

pulse width modulated, into a continuous analog signal and the circuit consist in a low pass filter. The main requirement is to provide a range of 0-5 V for the continuous signal when the duty-cycle of the digital output varies from 0-100% and the ripple in the reference to be low, so the influence on the PI current controller to be low.

3.5 Protection of the power switches

In order to switch safely during normal operation, without risk of destroying the switches due to the overvoltages caused by the leakage inductance of the transformer, a clamp circuit has to be employed. Furthermore, the shutdown of the converter during faulty situation is not a problem anymore, if the capacitance in the clamp circuit is sized in order to take over the energy in the PP converter magnetics (inductor and transformer) without exceeding the maximum admissible voltage.

-both switches on:

$$(L_{choke} + L_{trafo}) \cdot \frac{\left[I_{max} + \frac{\Delta I_{ripp}}{2}\right]^2}{2} = \frac{1}{2} C_{damp} \left(U^2_{max-MOS} - U^2_{max-damp}\right) \quad (3.1)$$

-a single switch on:

$$(L_{choke} + L_{trafo}) \cdot \left[I_{max} + \frac{\Delta I_{ripp}}{2}\right]^2 = \frac{1}{2} C_{damp} \left(U^2_{max-MOS} - U^2_{max-damp}\right) \quad (3.2)$$

where L_{choke} is the inductance of the PP inductor, L_{trafo} is the leakage inductance of the transformer, I_{max} is the average current from the FC, ΔI_{ripp} is the current ripple in the FC unfiltered current, C_{damp} is the capacitance of the clamp circuit, $U_{max-MOS}$ is the maximum admissible voltage across the power devices and $U_{max-damp}$ is the maximum voltage in the clamp circuit in normal operation, given by the load of the clamp circuit.

The second case is also the most severe. Therefore, the value of the capacitor is found by replacing the parameters with the quantities from the PP converter design: $L_{choke} = 28$ μH, $L_{trafo} = 0.5$ μH, $I_{max} = 40$A, $\Delta I_{ripp} = 10$ A, $U_{max-MOS} = 190$ V, $U_{max-damp} = 175$V, which gives $C_{damp} > 10.5\mu$F / 200Vdc and a current capability higher than 45 Amps.
It has been chosen a 20uF/250Vdc film capacitor (PHE426), with $dU/dt = 30\text{V}/\mu\text{s}$ which gives a current capability of 600A.

3.6 Adaptive load for the clamp circuit

The energy, which flows in the clamp circuit capacitor during normal operation, depends only on the leakage inductance of each primary winding, and is dependent on load condition. As a high internal resistance characterizes the characteristic of the fuel cell, it is expected that the power flow in the clamp circuit will increase drastically, when the operating point

is getting close to the maximum power. This depends on the leakage inductance of the half split primary winding of the transformer L_{trafo}, on the value of the switching frequency f_{sw} and on the current, which is braked.

$$P_{clamp} = 2f_{sw}\frac{L_{trafo}}{2}\left[\frac{I_{FC} + \frac{\Delta I_{ripp}}{2}}{2}\right]^2 \tag{3.3}$$

Requirements for the adaptive load in the clamp circuit are to limit the voltage level in order to provide safe operation for the switches and also to maintain a higher voltage in the clamp capacitor, which will force a faster turn-off and therefore lower switching losses and also keep the clamp circuit blocked from working as a rectifier when the voltage across the primary reflects the conduction of the diode rectifier in the secondary winding. Therefore, the voltage in the clamp circuit should be maintained high in a wide range of power levels. Experiments on the prototyped transformers are carried out by adapting the value of the load in order to maintain the voltage in the clamp capacitor at a desired value is shown in Fig. 3.5. The load consists in a variable resistor to feed back energy in the fuel cell, with a maximum value of 8.8 kΩ, which may be decreased in order to increase consumption. All the operating range is checked and the results are presented below.

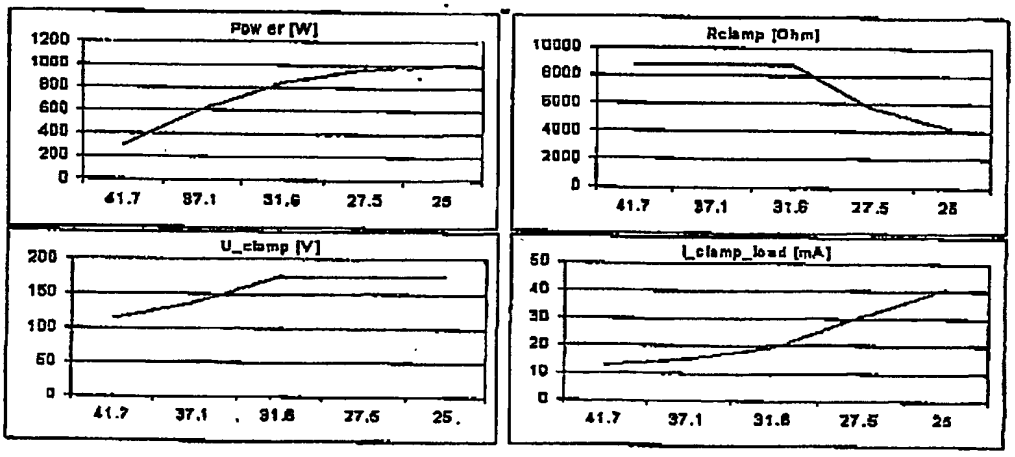


Figure 3.5: *Required load for the clamp circuit determined by experiments on the chosen transformer.*

An ideal characteristic of the load for the clamp circuit is presented in Fig 3.6 and the practical implementation is depicted in the right side.

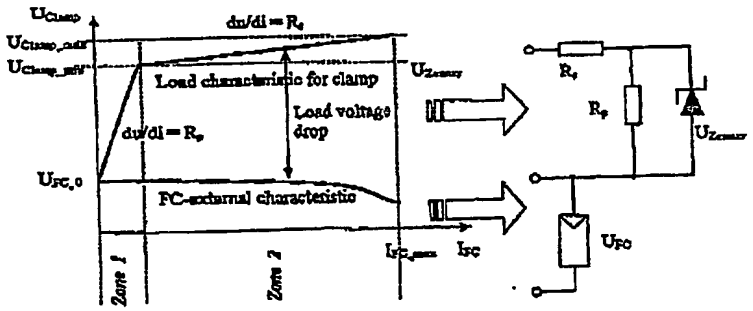


Figure 3.6: *Ideal characteristic of the load for the clamp circuit and the practical implementation.*

The meaning of the elements in the circuit: The Zenner diode is necessary to ensure that the load will work only for voltage levels higher than the reflected voltage from the secondary side and below the maximum allowable voltage. At low power, it is necessary to by-pass the Zenner diode with a parallel resistor R_p, in order to discharge the clamp capacitor, as well as to decrease the power dissipation in the Zenner diode at higher voltage drop level.

A series resistance R_s is necessary to adapt the external characteristic of the fuel cell. The limit for the regulation voltage of the Zenner diode are verified:

$U_{Zenner} > 2U_{DC}/n_{trafo} - U_{FCmin}$, which gives a minimum limit of 75 V
$U_{Zenner} < U_{max} - U_{FCmin}$, which gives a maximum limit of 150 V.

It is chosen $U_{Zenner} = 120$ V and in order to provide the necessary power dissipation ($I_{loadmax}$ = 45 mA), a group of +3xgV/1n Zenner diodes is chosen. Also $R_p = 15$ kΩ provides a low consumption in the low power range and is able to discharge the clamp capacitor in a satisfactory time period. The series resistor R_s is chosen of 200 Ohm in order to fulfill the following equation:

$$R_s = (U_{max} - U_{Zennermax} - U_{FCmin})/I_{loadmax} \tag{3.4}$$

The experimental evaluation of the prototype confirmed a good matching of the voltage in the clamp circuit with the characteristic of the transformer.
Because the energy from this load applied to the clamp circuit is wasted, it has been introduced a circuit which uses a part of this energy to feed a small fan for cooling of the power transformer of the PP converter. A comparator senses when the amount of energy

in the clamp circuit which is proportional to the FC current increases, which means that the power processed by the PP converter increases and losses in the transformer increases. Then the fan is supplied and starts cooling the transformer. The overall efficiency of the PP is not affected. This is shown in Fig. 3.7.

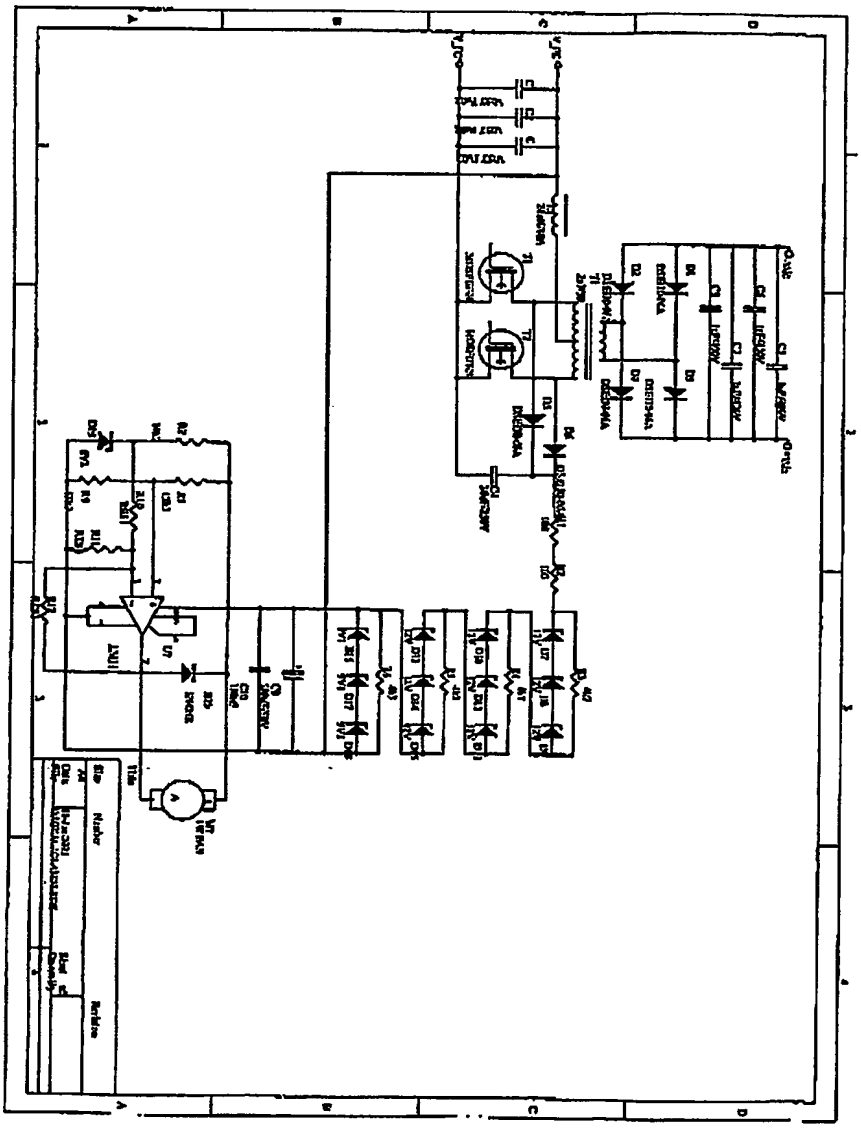


Figure 3.7: *Clamp circuits*

Chapter 4

Testing the Current Fed Push Pull Converter

TEST RESULTS the first prototype of the current fed DC-DC converter are shown. Steady state operation will be presented and a procedure to start up the converter without triggering the over current protection due to inrush current. Losses will be analysed before the efficiency is evaluated.

4.1 Steady state operation

Steady state operation is demonstrated with a ohmic load of the converter. Fig 4.1 on the next page shows steady state waveforms at different power levels. It should be noted that the output current is negative due to the positive direction of the current probe. The waveforms match those shown by simulation earlier. The figure illustrates how the switch over voltage during commutation increases with the inductor current(and power level) due to the increased amount of stored energy in the leakage inductance in the transformer. But the obtained magnectic coupling between the two primary windings is quite high as the switch current is balanced (ie. the windings shares the current equally).

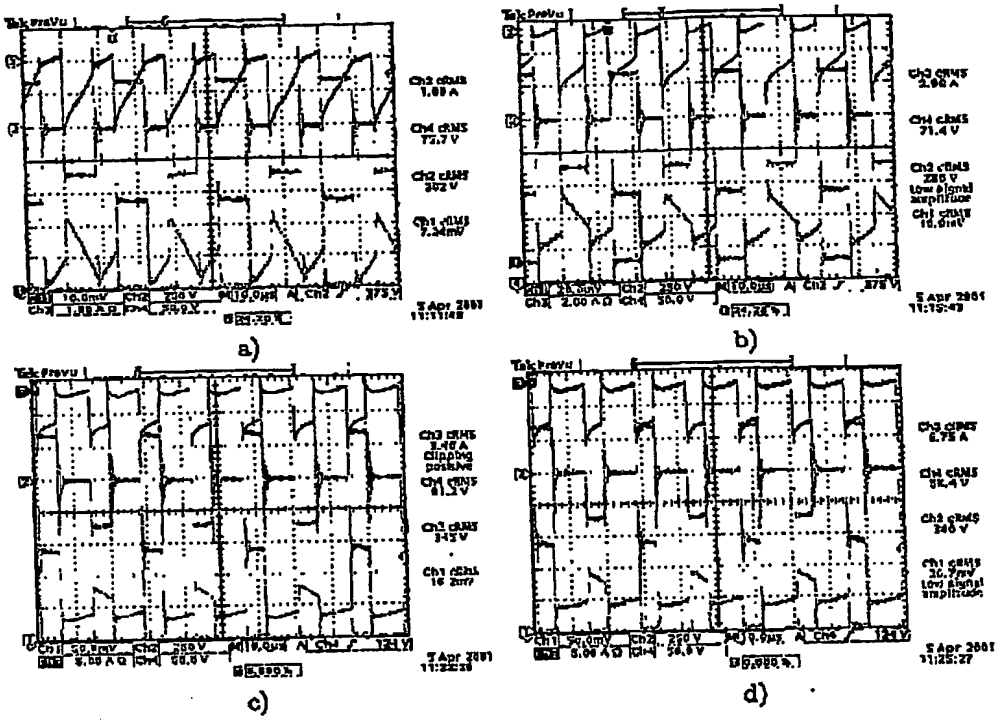


Figure 4.1: *Measured steady state waveforms of the current fed push pull converter. Magenta: output current, blue: secondary transformer voltage, green:switch voltage and yellow: switch or primary transformer winding current. a) 300W, b) 600W, c) 966W and d) 1000W.*

4.2 Startup

Startup is not as straight forward as it seems because of the boost nature of the circuit. Hence, there is no reflecting voltage to decrease the inductor current and the current is therefore not controllable - in current mode. Therefore a soft startup procedure have been developed (cf. chapter 3). Fig. 4.2 on the facing page shows a whole startup of the current fed push pull converter: The two top signals shows the two gate signals, the middle signal is the clamp voltage and the bottom is the inductor current. The transition from voltage mode to current mode can easily be identified as the point where there is a sudden change in the inductor current -about one division before the middle of the screen(time scale).

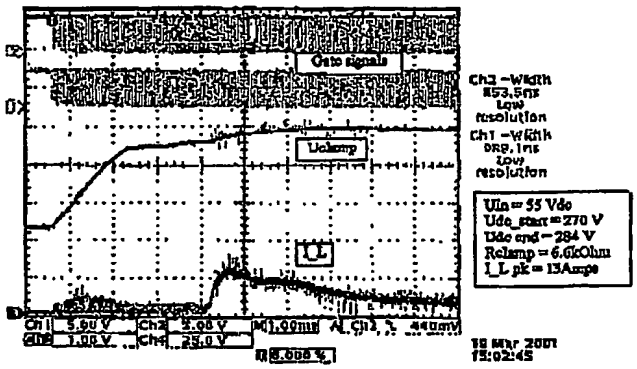


Figure 4.2: *Startup of the current fed push-pull converter.*

Fig. 4.3 shows a zoom of the transition from voltage mode to current mode. From this figure is can be seen how the gate signals change at the point of transition. Before the transition (in voltage mode) the converter operates (seen from the inductor) as a buck converter with a near unity duty cycle and just after the transition (current mode) the converter operates as a boost converter with a low duty cycle. Thus, the transition is a chance from buck mode operation to boost mode operation.

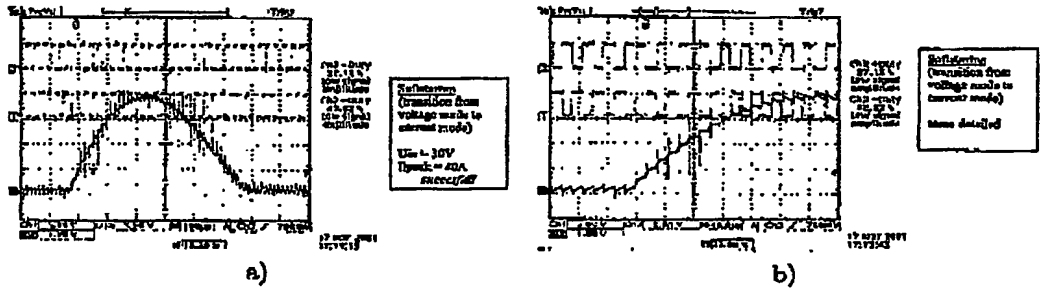


Figure 4.3: *Measured transition from voltage mode control to current mode control.*

4.3 Losses and efficiency

Fig. 4.4-4.5 shows measured losses for the current fed push pull converter with the final transformer. Fig. 4.6 shows the loss distribution. It can be seen that the dc-dc converter

has a relative high efficiency up to 600W and even around 91-92% at full power. In addition, these figures clearly shows the power loss in the clamp circuit.

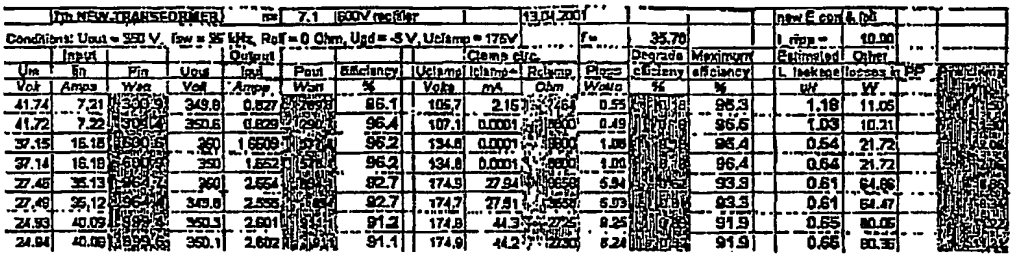


Figure 4.4: *Losses and efficiency at different power levels with the designed transformer.*

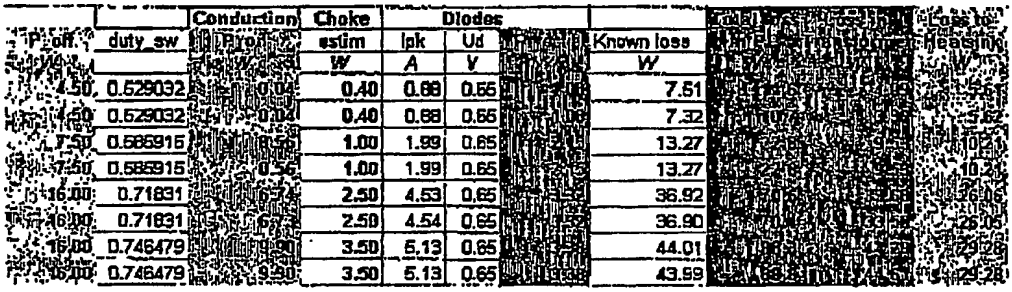


Figure 4.5: *Losses and efficiency at different power levels with the designed transformer.*

4.4 Conclusion

This chapter has demonstrated the functionality of the current fed push pull converter and the modified startup procedure has been verified. Losses and efficiency have been measured and the converter has an efficiency in the desired range to meet the target efficiency. Thus, the current fed push pull converter operates as expected and the efficiency also corresponds to the specifications.

4.4. Conclusion

	Loss distribution
	MOS COND MOS OFF TOTAL
300W / 350Vout	
300W / 350Vout	
300W / 350Vout	
300W / 350Vout	
300W / 350Vout	
300W / 350Vout	
1000W / 350Vout	
1000W / 350Vout	

Figure 4.6: *Loss distribution at different power levels.*

75

Chapter 5

Inverter control and modulation

THIS CHAPTER describes the implemented control and modulation of the grid connected inverter. Special attention is put on control of the grid current and on the grid connected LCL filter.

5.1 Requirements

The aim of the inverter control is to load the DC-link capacitor in order to maintain the dc-component of the link voltage at the desired value $V_{dc,ref}$. The current impressed into the utility grid must comply with EMC regulations - both low frequency and high frequency. In addition, the inverter must be fast enough to protect the dc-link and the semiconductors from over voltages due to power processing from the push-pull converter. In short,

DC-link voltage control: The DC-link voltages must be controlled to have a dc-value at $V_{dc,ref}$.

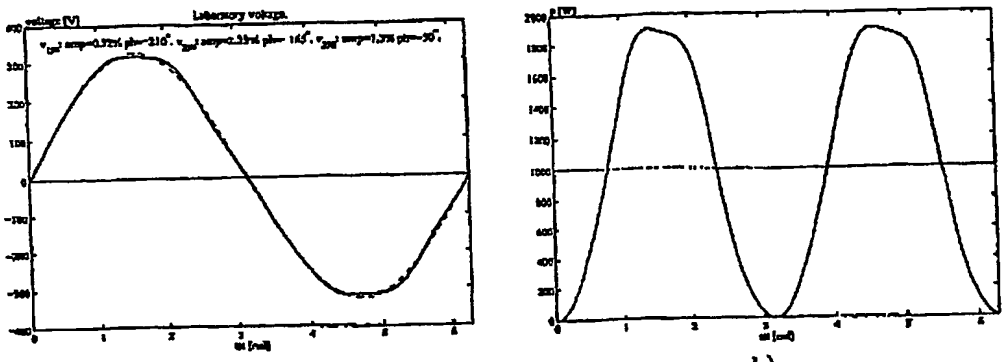
Grid current waveform: The grid current must comply with IEC-61000-3-2. In addition, the current controller must be robust towards line voltage background distortion. A sample from the laboratory is seen in fig. 5.1 on the next page.

Besides the harmonic content of the line current, two performance indexes are used:

$$\%THD_i \triangleq 100 \times \frac{\sqrt{I_g^2 - I_{g,1}^2}}{I_{g1}} = 100 \times \sqrt{\sum_{h \neq 1} \left(\frac{I_{g,h}}{I_{g,1}}\right)} \tag{5.1}$$

$$PF \triangleq \frac{P_g}{S_g} = \frac{\sum V_{g,h} I_{g,h} \cdot \cos(\phi_h)}{V_g I_g} \tag{5.2}$$

$$= \frac{I_{g,1}}{I_g} \cdot \cos(\phi_1) \qquad \text{for sinusoidal voltage} \tag{5.3}$$



a) b)

Figure 5.1: *Background line voltage distortion. a) Laboratory voltage including third, fifth, and seventh harmonic voltage. b) Line power with distorted voltage and perfect resistor emulation.*

The total harmonic current distortion $\%THD_i$ is a relative measure of the degree of distortion of the line current to the first harmonic current. With perfect resistor emulation and with a background distorted line voltage, the line current $\%THD_i$ will the same as the line voltage distortion $\%THD_v$. The measured total harmonic line voltage voltage distortion is around 3.5%. The power factor PF is a measure of the active power P_g to the apparent power S_g. For perfect resistor emulation and regardless of background distortion, the power factor will be unity. The power factor index also includes the phase angle between voltage and current.

5.2 Control strategy

There exist several methods/strategies to control the grid connected inverter. In order to fullfill the low harmonic regulation IEC 61000-3-2 and to limit the power losses in the inverter the converter is controlled to emulate a resistor R_e. Hence, the grid current waveform must be a scalar of the voltage waveform:

$$R_e = \frac{v_g}{i_g} \tag{5.4}$$

With perfect resistor emulation and with a grid voltage as in Fig. 5.1.a then the grid power will be as shown in Fig. 5.1.b. Shown in Fig. 5.2, the control strategy of the inverter consist of two cascaded control loops. The inner current lop shapes the line current to a shape similar to the line voltage. Hence, the inverter emulates a resistance. The amplitude of the

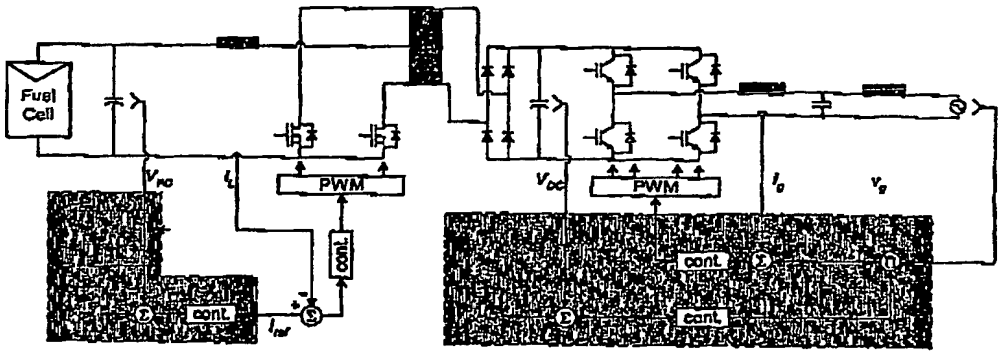


Figure 5.2: *Control strategy of the whole GPI converter.*

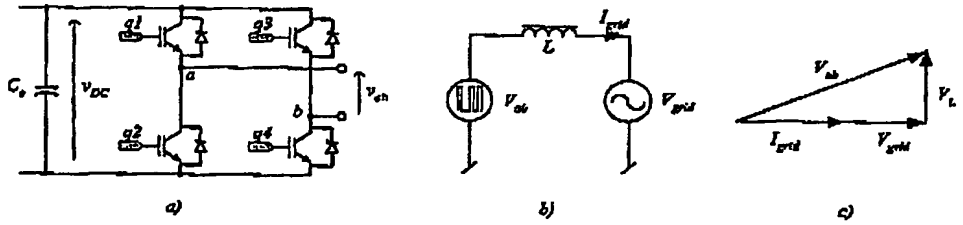


Figure 5.3: *Principle of current control. a) Inverter, b) equivalent circuit and c) phasor circuit.*

line current or the value of the emulated resistance is controlled by the outer voltages loop. Since the line current -in the ideal case- is sinusoidal the power delivered to the grid is a pulsating power at twice the line frequency and the power ripple is 100% (cf. fig. 5.1.b).

Fig. 5.3 shows the control principle of the line current. As will be shown later, the grid connected LCL filter can be regarded as a inductance(for low frequencies) and the equivalent circuit is shown in Fig 5.3.b and the corresponding phasor diagram for unity power factor operation

The voltage phasor equation becomes:

$$\vec{V}_{ab} = \vec{V}_{grid} + \vec{V}_L \tag{5.5}$$

Since the inverter voltage v_{ab} consist of the sum of the grid voltage and the inductor voltage the grid voltage is fed forward and only the inductor voltage is calculated by the current

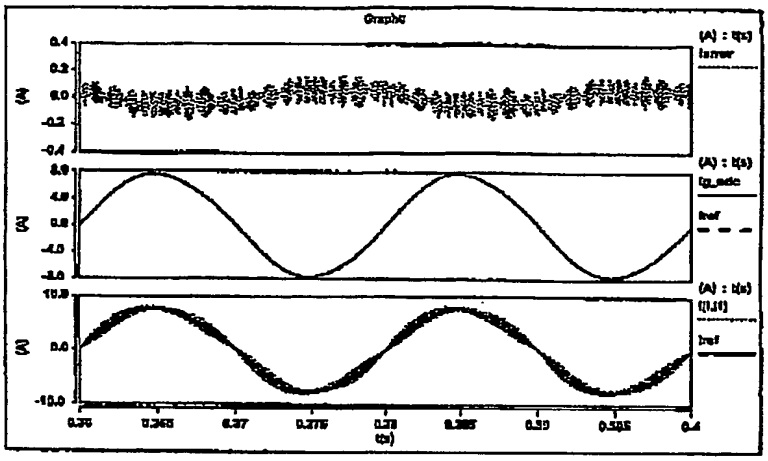


Figure 5.4: *Example of the current control loop.*

controller. Fig. 5.4 shows an example of this control strategy. The upper curve shows the error current, the middle curve shows the reference current and the lower plot shows the inductor current. The grid and the inductor current are not sinusoidal because the outer voltage control loop distort the current reference which the current controller follows (cf. the multiplier in fig. 5.2). As can be seen the inductor current follows the reference current and the error signal is low in amplitude relative to the reference.

5.3 Utility filter

From fig. 5.4 it is obvious that the grid current is a filtered version of the inductor current. As depicted in Fig. 5.5, a third order LCL line filter is used. Hence, the inductor current in fig. 5.4 thus corresponds to the current i_i through Z_i in fig. 5.5 and the current i_g through Z_g is the grid current.

The LCL filter has the following components (without damping):

$$Z_i = R_{Li} + L_i s \tag{5.6}$$

$$Z_g = R_g + L_g s \tag{5.7}$$

$$Z_0 = \frac{1}{Cs} \tag{5.8}$$

and the component values are listed in tab. 5.1.

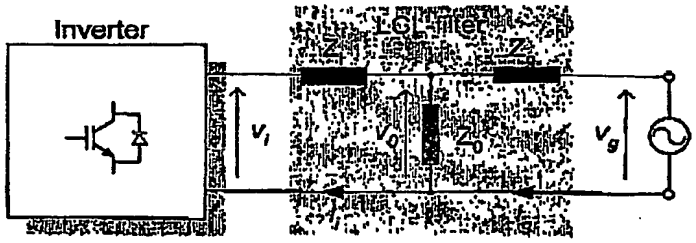


Figure 5.5: *Line filter configuration.*

L_i [mH]	R_i [mΩ]	L_g [μH]	R_g [mΩ]	C [μ F]
4.0	400	850	180	2.2

Table 5.1: *Line filter parameters. R_i and R_g are dc-values.*

5.4 Filter transfer functions

This section describes the transfer functions used in the later current control design. Therefore the aim is to link the filter terminal voltages(grid and inverter voltage) to the inductor currents.

5.4.1 The general Case

In the general case all passive elements are treated as impedances. Writing the two voltage equations yields:

$$\begin{array}{rcrr} V_i & = & (Z_i + Z_0)I_i & -Z_0 I_g \\ V_g & = & Z_0 I_i & -(Z_0 + Z_g)I_g \\ I_i & = & \frac{Z_0+Z_g}{Z_0} I_g & \frac{1}{Z_0} V_g \\ I_g & = & \frac{1}{Z_g+Z_0} Z_0 I_i & \frac{-1}{Z_g+Z_0} V_g \end{array} \tag{5.9}$$

Transfer function from V_i to I_g, ie. I_g/V_i (elimination of I_i):

$$\begin{aligned} V_i &= (Z_i + Z_0)\left(\frac{Z_0 + Z_g}{Z_0} I_g + \frac{1}{Z_0} V_g\right) - Z_0 I_g \\ &= \frac{Z_0(Z_i + Z_g) + Z_i Z_g}{Z_0} I_g + \frac{Z_0 + Z_i}{Z_0} V_g \end{aligned} \tag{5.10}$$

$$\Updownarrow$$

$$\begin{aligned} I_g &= \frac{Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g}\left(V_i - \frac{Z_0 + Z_i}{Z_0} V_g\right) \\ &= \frac{Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g} V_i - \frac{Z_0 + Z_i}{Z_0(Z_i + Z_g) + Z_i Z_g} V_g \end{aligned} \tag{5.11}$$

Transfer function from V_i to I_i, ie. I_i/V_i (elimination of I_g):

$$\begin{aligned} V_i &= (Z_i + Z_0) I_i - Z_0\left(\frac{1}{Z_g + Z_0} Z_0 I_i + \frac{-1}{Z_g + Z_0} V_g\right) \\ &= \left(\frac{Z_0(Z_i + Z_g) + Z_i Z_g}{Z_g + Z_0}\right) I_i + \frac{Z_0}{Z_g + Z_0} V_g \end{aligned} \tag{5.12}$$

$$\Updownarrow$$

$$\begin{aligned} I_i &= \left(\frac{Z_g + Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g}\right) V_i - \left(\frac{Z_g + Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g}\right) \frac{Z_0}{Z_g + Z_0} V_g \\ &= \frac{Z_g + Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g} V_i - \frac{Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g} V_g \end{aligned} \tag{5.13}$$

Thus eq. (5.11) and (5.13) gives the following general transfer functions:

$$H_{i \to g}(s) \triangleq \left.\frac{I_g(s)}{V_i(s)}\right|_{v_g(s)=0} = \frac{Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g} \tag{5.14}$$

$$H_{i \to i}(s) \triangleq \left.\frac{I_i(s)}{V_i(s)}\right|_{v_g(s)=0} = \frac{Z_0 + Z_i}{Z_0(Z_i + Z_g) + Z_i Z_g} \tag{5.15}$$

$$H_{g \to g}(s) \triangleq \left.\frac{I_g(s)}{V_g(s)}\right|_{v_i(s)=0} = -\frac{Z_g + Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g} \tag{5.16}$$

$$H_{g \to i}(s) \triangleq \left.\frac{I_i(s)}{V_g(s)}\right|_{v_i(s)=0} = -\frac{Z_0}{Z_0(Z_i + Z_g) + Z_i Z_g} \tag{5.17}$$

This are the four transfer functions linking the two filter terminal voltages (grid voltage and inverter voltage) to the two inductor currents. For the purpose of control the transfer functions of interest are $H_{i \to g}(s)$ and $H_{i \to i}(s)$. These two transfer functions will be used in the controller design. First the ideal case is analysed and then non-ideal conduction resistance is taken into account. It should be noted that $H_{i \to g}(s) = -H_{g \to i}(s)$ due to the symmetry of the filter and the sign inversion follows from the definition of current directions in Fig. 5.5.

5.4.2 The ideal case

Parasitic resistors are eluded in the ideal case. Setting $Z_i = L_i s$, $Z_g = L_g s$, $Z_0 = 1/(Cs)$ yields:

$$H_{i\to g}(s) \triangleq \left.\frac{I_g(s)}{V_i(s)}\right|_{v_g(s)=0} = \frac{1}{L_i L_g C s^3 + (L_i + L_g)s} \tag{5.18}$$

The amplitude response becomes:

$$|H_{i\to g}(j\omega)| = \frac{1}{\sqrt{(-L_i L_g C\omega^3 + (L_i + L_g)\omega)^2}} = \frac{1}{|(L_i + L_g)\omega - L_i L_g C\omega^3|} \tag{5.19}$$

Again, setting $Z_i = L_i s$, $Z_g = L_g s$, $Z_0 = 1/(Cs)$ yields:

$$H_{i\to i}(s) \triangleq \left.\frac{I_i(s)}{V_i(s)}\right|_{v_g(s)=0} = \frac{1 + L_g C s^2}{L_i L_g C s^3 + (L_i + L_g)s} \tag{5.20}$$

The amplitude response becomes:

$$|H_{i\to i}(j\omega)| = \sqrt{\left(\frac{L_g C\omega^2 - 1}{-L_i L_g C\omega^3 + (L_i + L_g)\omega}\right)^2} = \left|\frac{L_g C\omega^2 - 1}{(L_i + L_g)\omega - L_i L_g C\omega^3}\right| \tag{5.21}$$

The resonance frequency of the LCL filter is

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{L_i C L_g}} \approx 4kHz \tag{5.22}$$

Fig. 5.6 shows the amplitude response of $|H_{i\to g}(j\omega)|$, $|H_{i\to i}(j\omega)|$ and for $|H_{tr}(j\omega)|$ where $|H_{tr}(j\omega)|$ is the amplitude response of a first order system consisting of an inductance (inner) and the parasitic conduction resistance.

As can be seen, the the amplitude response is almost equal for all three functions when the frequency is lower than the resonance frequency.

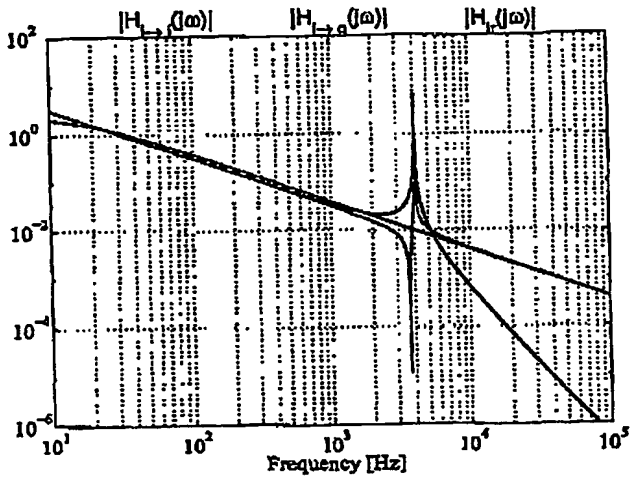


Figure 5.6: *Amplitude response of ideal LCL filter and for a LR circuit.*

5.4.3 The non-ideal case

Defining $Z_t = Z_i + Z_g$ with $L_t = L_i + L_g$ and $R_t = R_i + R_g$ and setting $Z_i = L_i s + R_i$, $Z_g = L_g s + R_g$, $Z_0 = (Cs)^{-1}$ yields:

$$H_{i\to i}(s) = \frac{s^2 L_i C + s R_i C + 1}{s^3 L_i L_g C + s^2 (C L_i R_g + C L_g R_i) + s (L_t + R_i R_g C) + R_t} \tag{5.23}$$

$$H_{i\to i}(j\omega) = \frac{j\omega R_i C + [1 - \omega^2 L_i C]}{j[\omega (L_t + R_i R_g C) - \omega^3 L_i L_g C] + [R_t - \omega^2 (C L_i R_g + C L_g R_i)]} \tag{5.24}$$

and

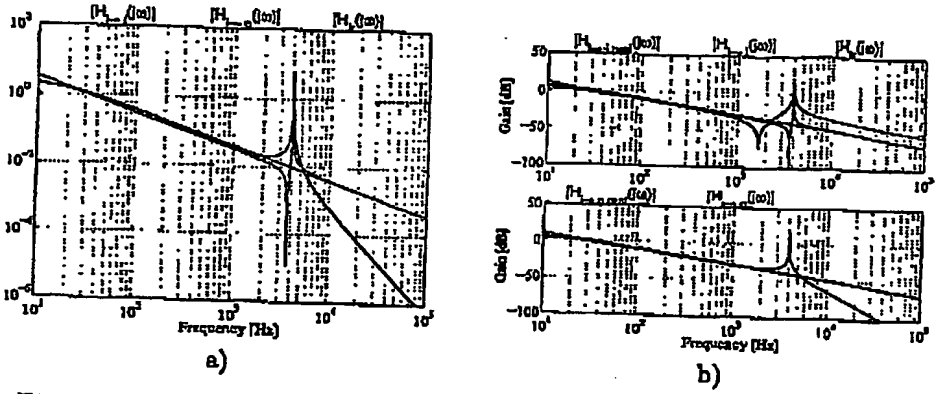
$$H_{i\to g}(s) = \frac{1}{s^3 L_i L_g C + s^2 (C L_i R_g + C L_g R_i) + s (L_t + R_i R_g C) + R_t} \tag{5.25}$$

$$H_{i\to g}(j\omega) = \frac{1}{j[\omega (L_t + R_i R_g C) - \omega^3 L_i L_g C] + [R_t - \omega^2 (C L_i R_g + C L_g R_i)]} \tag{5.26}$$

The amplitude responses becomes:

$$|H_{i\to i}(j\omega)| = \sqrt{\frac{(\omega R_i C)^2 + [1 - \omega^2 L_i C]^2}{[\omega (L_t + R_i R_g C) - \omega^3 L_i L_g C]^2 + [R_t - \omega^2 (C L_i R_g + C L_g R_i)]^2}} \tag{5.27}$$

$$|H_{i\to g}(j\omega)| = \frac{1}{\sqrt{[\omega (L_t + R_i R_g C) - \omega^3 L_i L_g C]^2 + [R_t - \omega^2 (C L_i R_g + C L_g R_i)]^2}} \tag{5.28}$$



a) b)

Figure 5.7: *Amplitude response of LCL filter. a) Comparison of the different transfer functions. b) Comparison between the ideal cases without series conduction resistance and the non-ideal case including these resistors.*

Fig. 5.7 shows the amplitude responses when parasitic conducting resistance is included and in fig. 5.7.b a comparison between each of the amplitude responses with and without parasitic conducting resistance is shown.
In order to improve the stability of the current loop damping of the filter can be utilized (will be shown later). This will be treated in the next section.

5.4.4 Adding passive damping in parallel to Z_g

Filter transfer functions are derived when passive damping of the outer inductor is introduced.

Ideal case: Parasitic conducting resistors are omitted. Setting $Z_g = L_g s \| R_d$ yields

$$Z_g = L_g s \| R_d = \frac{L_g s R_d}{L_g s + R_d} \tag{5.29}$$

The filter transfer function then becomes

$$H_{i \to i}(s) = \frac{Z_0 + Z_i}{Z_0(Z_i + Z_g) + Z_i Z_g} = \frac{\frac{1}{sC} + L_i s}{\frac{1}{sC}\left(L_i s + \frac{L_g s R_d}{L_g s + R_d}\right) + L_i s \frac{L_g s R_d}{L_g s + R_d}} \tag{5.30}$$

$$= \frac{L_i L_g C s^3 + L_i C R_d s^2 + L_g s + R_d}{L_i L_g C R_d s^3 + L_i L_g s^2 + R_d(L_i + L_g)s} \tag{5.31}$$

Non ideal case: Parasitic conduction resistors are included.
The filter transfer function becomes:

$$H_{i\to i}(s) = \frac{Z_0 + Z_i}{Z_0(Z_i + Z_g) + Z_i Z_g} \tag{5.32}$$

$$= \frac{\frac{1}{sC} + L_i s + R_i}{\frac{1}{sC}\left(L_i s + R_i + \frac{R_g(L_g s + R_d)}{L_g s + R_g + R_d}\right) + (L_i s + R_i)\left(\frac{R_d(L_g s + R_g)}{L_g s + R_g + R_d}\right)} \tag{5.33}$$

$$= \frac{(L_i C s^2 + R_i C s + 1)(L_g s + R_g + R_d)}{(L_i s + R_i)(L_g s + R_g + R_d) + R_d(L_g s + R_g) + C s R_d(L_g s + R_g)(L_i s + R_i)} \tag{5.34}$$

$$= \frac{s^3 a_3 + s^2 a_2 + s a_1 + a_0}{s^3 b_3 + s^2 b_2 + s b_1 + b_0} \tag{5.35}$$

where

$$\begin{aligned} a_3 &= L_i L_g C & b_3 &= L_i L_g C R_d \\ a_2 &= L_i C(R_g + R_d) + L_g R_i C & b_2 &= R_d C(L_g R_i + L_i R_g) + L_i L_g \\ a_1 &= L_g + C R_i (R_g + R_d) & b_1 &= C R_d R_g R_i + L_g R_d + L_i(R_g + R_d) + L_g R_i \\ a_0 &= R_g + R_d & b_0 &= R_g + R_i R_d \end{aligned} \tag{5.36}$$

5.4.5 Summary

Transfer function have been derived of the LCL filter for the purpose of current control. A comparison between these third order functions and a inductive equivalent shows that below the resonance frequency the single inductor-resistor equivalent is an adequate approximation of the inverter voltage to inverter current but in order to describe/analyse stability the LR circuit is not adequate near the resonance frequency of the LCL filter.

5.5 Current loop design

This section describes the design of the current control loop.

Control loop structure

Fig. 5.8 shows the block diagram of the current control loop. The input reference is the inverse of the emulated resistance $R_e(z)$ (cf. Eq. (5.4)). The emulated conductance $g_e(z) \triangleq R_e^{-1}(z)$ is multiplied with the grid voltage in order to form the current reference. If a compensation technique (to be explained later) is used then $C_{xp}(z)$ manipulates the reference to change the system dynamics between I_i/I_{ref}. If this compensation is not used then $C_{xp}(z) = 1$. Hence, if $C_{xp}(z) = 1 \Rightarrow I_{ref,comp}(z) = I_{ref}(z)$. The output/inverter

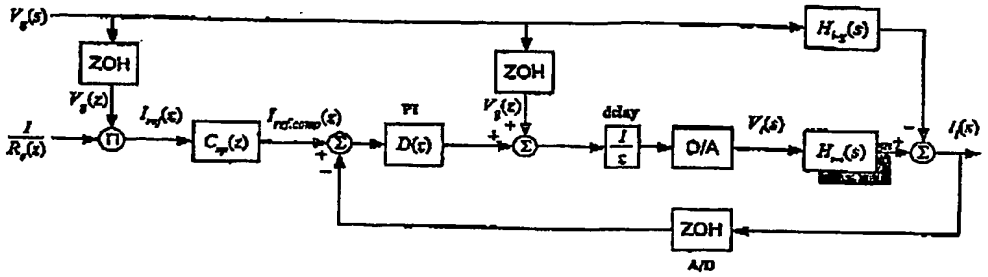


Figure 5.8: *Control block diagram for the current loop.*

voltage $V_i(s)$ to the system $H_{i\to i}(s)$ is the sum of the current controller $D(z)$ and the feedforward of the grid voltage $V_g(z)$. According to Eq. (5.13) the inductor current should be a summation of the inverter voltage and the grid voltage filtered through Eq.(5.15) and Eq. (5.17) respectively. Utilizing the symmetry of these filter transfer functions ($H_{g\to i}(s) = -H_{i\to g}(s)$) allows to substitute $H_{g\to i}(s)$ by $-H_{i\to g}(s)$ as can be observed. Fig. 5.7.a reveals that a frequencies well below the filter resonance frequency ($f \ll f_{res}$) then $|H_{i\to g}(j\omega)| \approx |H_{i\to i}(j\omega)|$ which is also true for the phase margin (this can also be seen by comparing Eq. (5.27) and Eq. (5.27)). Thus, the feedforward of the grid voltage cancels the influence from the grid voltage (at low frequencies). But it is also obvious that the feedforward loop has less attenuation at higher frequencies and is thus not immune towards high frequency noise. Therefore a low pass filtering of the feedforward loop should be used in order to avoid noise problems.

Current control loop specifications

Design of the current controller will be done based on both the third order LCL transfer function and on the simple LR model. The basic demands to the current control loop is (besides stability)

1. The current controller must be able perform a near perfect resistor emulation which means a near unity power factor operation with a low current thd.
2. The steady state error should ideally be zero but at least as small as possible. The term steady state is used for the situation where the emulated resistance is constant.

In order to obtain a high power factor and a low current thd the current controller must be able to track not only the fundamental grid frequency at 50 Hz but also the distortion components such as shown in fig.5.1.a on page 76. The switching frequency and the sampling frequency is 10 kHz with a time period at 100 μs. In order to handle background

distortion the settling time of the current controller is set to $X = 10$ samples witch yields 1ms. Setting the damping ratio to $\zeta = \frac{1}{\sqrt{2}} \approx 0.707$ provides optimal step response in terms of settling time. Hence the desired placement of the dominating poles is

$$s_{1,2} = -\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2} = \frac{\omega_n}{\sqrt{2}}(-1 \pm j) \tag{5.37}$$

$$= \frac{2\pi}{\sqrt{2}XT_s}(-1 \pm j) = \frac{\sqrt{2}\pi}{XT_s}(-1 \pm j) \approx 4442.75(-1 \pm j) \tag{5.38}$$

$$z_{1,2} = \exp(T_s s_{1,2}) = \exp\left(\frac{\sqrt{2}\pi}{X}(-1 \pm j)\right) \approx 0.579 \pm j0.276 \tag{5.39}$$

Hence, a natural frequency at $\omega_n = \frac{2\pi}{XT_s} \approx 6283$ [rad/s].

Type of current controller

Choosing the type of controller depends on the type of system and on the type of reference signal. The type of system is determined as the number of pure integrators of the open loop including the controller. Thus a I-controller will increase the type of system by one. Ideally, the current controller must be able to follow a AC-signal as reference. Both the simple LR model and the third order LCL model including damping and parasitic conducting resistors are type zero systems meaning that there are no pure integrators.

If a sine wave is regarded as a ramp reference signal then system must be type 2 system in order to have zero steady state error. A type 1 system will have a finite error. From this point of view a type 2 system should be selected but since the filter is a type 0 system two additional integrators must be added which in terms of stability is very difficult to handle. Since the settling time is much higher than then fundamental grid frequency the system can approximately be regarded as operating in quasi steady state with step inputs and a type 1 system have zero steady state error towards step input reference signals. Therefore,

- A PI controller is selected as current controller.
- The PI current controller will have a finite steady state error which decreases as the proportional gain increases.
- Roughly, the integrational part determines the phase shift between the grid voltage and current, and the proportional gain determines the reference signal tracking ability.

5.5.1 Simple LR equivalent model

The discrete transfer function of the $L_i s + R_i$ impedanze is

$$H_{lr}(s) = \frac{1}{L_i s + R_i} = \frac{1}{R_i} \cdot \frac{R_i/L_i}{s + R_i/L_i} \tag{5.40}$$

$$H_{lr}(z) = \frac{z-1}{z} Z\left\{\frac{H_{lr}(s)}{s}\right\} \tag{5.41}$$

$$= \frac{1 - \exp(-\frac{R_i}{L_i}T_s)}{R_i} \cdot \frac{1}{z - \exp(-\frac{R_i}{L_i}T_s)} = \frac{1-\alpha}{R_i} \cdot \frac{1}{z-\alpha} \tag{5.42}$$

where $\alpha \triangleq \exp(-\frac{R_i}{L_i}T_s)$. The PI controller transfer function:

$$D(z) = K_p \frac{z\left(1 + \frac{T_s}{T_i}\right) - 1}{z - 1} \tag{5.43}$$

The open loop transfer function (without delay):

$$GH_{-d}(z) = K_p \left(\frac{1-\alpha}{R_i}\right) \cdot \frac{z\left(1 + \frac{T_s}{T_i}\right) - 1}{(z-1)(z-\alpha)} \tag{5.44}$$

and including the delay

$$GH_{+d}(z) = K_p \left(\frac{1-\alpha}{R_i}\right) \cdot \frac{z\left(1 + \frac{T_s}{T_i}\right) - 1}{(z-1)(z-\alpha)z} = K_p \left(\frac{1-\alpha}{R_i}\right) \cdot \frac{z\left(1 + \frac{T_s}{T_i}\right) - 1}{z^3 - (1+\alpha)z^2 + \alpha z} \tag{5.45}$$

Fig. 5.9.a shows the root locus for this system in including delay. Left (Fig. 5.9.a) shows the influence on the root locus when the integration time T_i varies. In order to have a locus passing the desired pole placements a integration time $T_i = 8 \cdot T_s$ have been chosen. Fig. 5.9.b shows the root locus for $T_i = 8 \cdot T_s$.

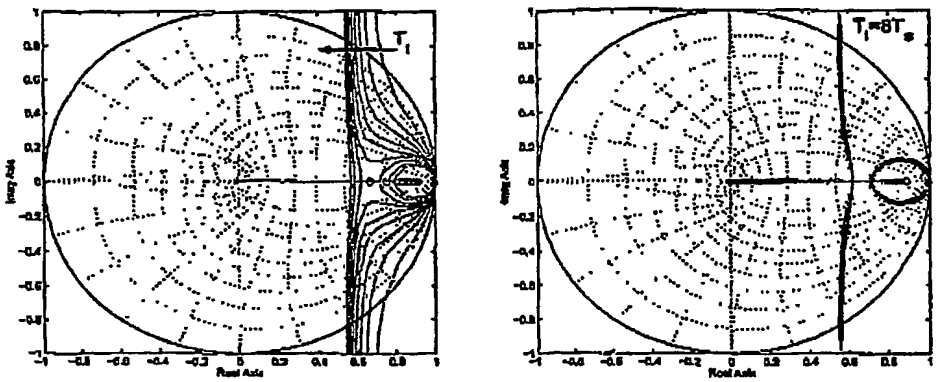


Figure 5.9: *Root locus of current loop including delay. a) Different integration times and b) root locus at $T_i = 8T_s$.*

Poles	Zeros	K_p	T_i/T_s
0.8333	0.8889	14	8
$0.5784 \pm j0.2888$			

Table 5.2: *System poles and zeros of the current control loop.*

At a proportional gain at $K_p = 14$ the poles and zeros of the closed loop is listed in table 5.2. Fig. 5.10.a shows step the response of the current control system (red) and the desired step response (blue). The dynamics are a bit different to the specified performance due the the extra pole added from the unit delay. The real pole and the real zero can be compensated in order to make the dynamics match the specifications:

$$C_{zp}(z) = \frac{1-n}{1-p} \cdot \frac{z-p}{z-n} = K_c \frac{1-nz^{-1}}{1-pz^{-1}} \tag{5.46}$$

Fig. 5.10.b shows the step response with compensation but also the effect of not compensating correctly. Thus in order to utilize compensation it is required to match the system poles and zeros exactly.

5.5.2 Complete *LCL* model

Analysing stability of the current loop with the third order LCL model it is necessary to include damping or some equivalent manipulation of the open loop poles at unity propor-

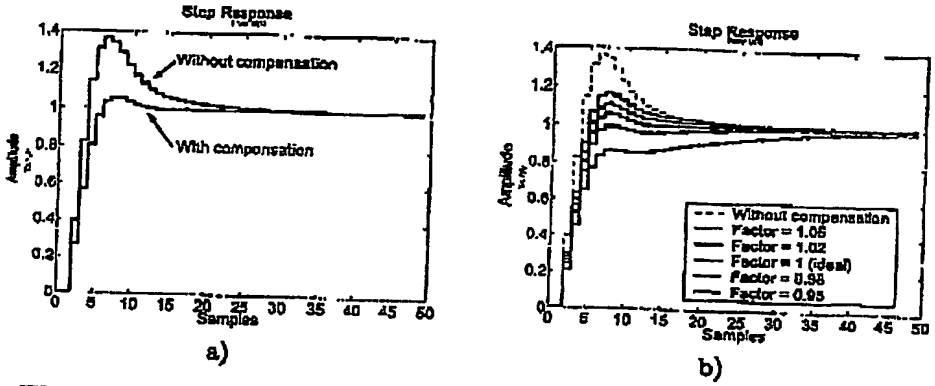


Figure 5.10: *Step response of current loop. a) with and without compensation and b) robustness of the compensation accuracy.*

tional gain. Here passive damping with a resistor in parallel to the outer/grid connected inductor is used. Fig. 5.11 shows the effect of adding damping in terms of stability.

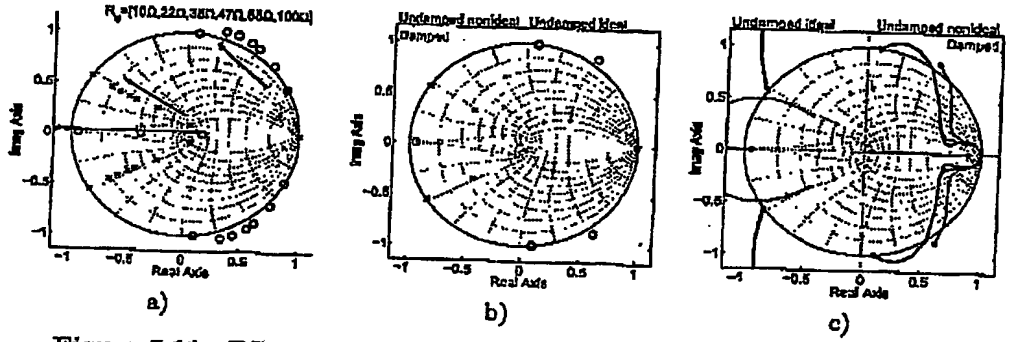


Figure 5.11: *Effects on open loop poles when passive adding damping. a) different damping resistors, b) R_d =38 Ω and c) root locus with and without damping resistor (38 Ω).*

Fig. 5.11.a shows open loop poles and zeros without (black) damping and the system poles (red) and zeros (blue) with different damping values. Of course as the damping resistor increases the poles and zeros moves towards the undamped positions. It can be observed that the open loop poles without damping are placed very close to the border of stability.

Using fig. 5.11.a alone it would be reasonable to choose the damping resistor as low as possible. But since the power dissipation in the damping resistor increases and filter attenuation decreases as the resistor value decreases there exist a trade off between stability, efficiency and filter attenuation. Tab. 5.3 shows simulated power dissipation in the damping resistor for different resistor values at different power levels.

Power [W]	Damping resistor [Ω] 10	22	38	47	68
300	1.269	0.668	0.399	0.324	0.225
$\Delta\eta$ [%]	0.432	0.223	0.133	0.108	0.075
600	1.307	0.686	0.410	0.333	0.231
$\Delta\eta$ [%]	0.218	0.114	0.068	0.055	0.039
1000	1.408	0.731	0.435	0.353	0.245
$\Delta\eta$ [%]	0.141	0.073	0.044	0.035	0.025

Table 5.3: *Power dissipation in damping resistor for different resistor values and at different power levels.*

Included in the table is the effect on the system efficiency. Fig. 5.12 shows an example on the current through and the power dissipated in the damping resistor. A damping resistor at $R_d = 38\Omega$ has been choosen and will be used throughout this chapter.

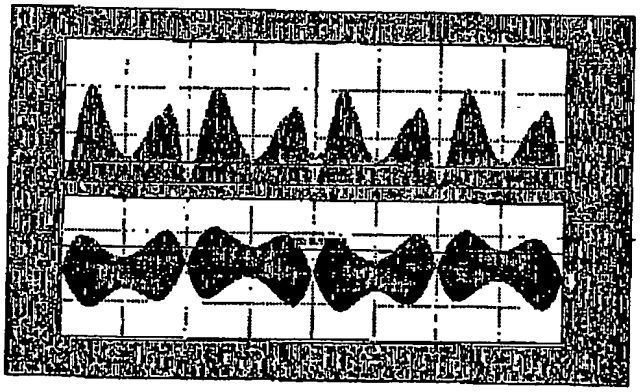


Figure 5.12: *Current and power dissipation in damping resistor at 600W and the damping resistor is 38Ω.*

Fig. 5.11.c shows the root locus with ($R_d = 38\Omega$) and without damping. It is obvious that

without damping the system is unstable and that the damping resistor stabilize the system.

Figure 5.13 shows root locus and step response when the lcl model in Eq. (5.31) is used. Three different integral time constants have been used. Fig 5.13.a shows the root locus with $T_i = 22T_s$ and the pole location for a proportional gain at $K_p = 11$ is shown. This gain shows to provide the best step response with $T_i = 22T_s$. Shown in fig. 5.13.b the step response has the same effects as shown in fig. 5.10.a (blue) since the overshoot tend to be higher than expected and the settling time is also longer than specified. Again, the responses can be improved by adding a compensation function similar to the one used for the simple LR model. Further more, the step responses in fig. 5.13.b,d,f are more oscillatory due to the additional poles near the stability border in the left part of the plot. In fig. 5.13.e-f are the root locus and step response with the same controller parameters as used for the simple LR model. The response is similar but more oscillatory. It should be noted that the dominating poles are slower in fig. 5.13.e than in fig. 5.9.b due to the more accurate model. Actually is not possible to obtain a much faster system and still maintain a stable system. Which of these three controller parameters to be used in the laboratory setup will be chosen through simulation in SABER (see section 5.8 on page 98).

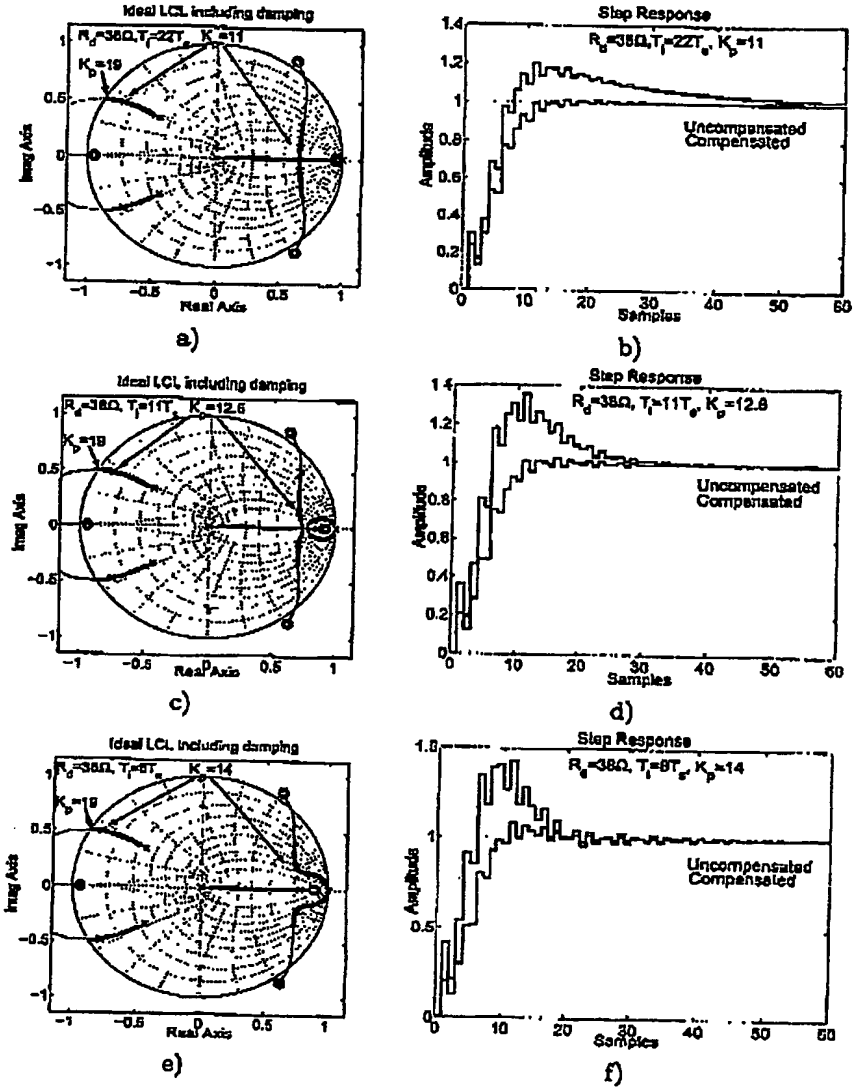


Figure 5.13: *Root locus and step response of current loop when the LCL model is used.*

5.6 Voltage loop design

As demonstrated in the previous section, the current controller controls the wave shape of the line current. The dc-link voltage is controlled by varying the amplitude of the grid current i_g. The dc-link voltage must be maintained on a level above the peak of the line current in order to be able to maintain controlability of the inverter. Regarding the bandwidth of the voltage controller there is a trade off between grid current reference distortion and dc-link over voltage protection: The grid current reference is basically formed as the dc-link current reference multiplied by the measured grid voltage which means the that the the grid current reference will only be a scalar replica of the grid voltage in the case of a constant dc-link current reference. This requires a very slow dc-link control. In terms of dc voltage protection the dc voltage controller must be fast enough to avoid hazardous operation. Actually hazardous operation will not be reached due to the hardware protection, but the dc-link controller must be fast enough to avoid triggering the hardware protection which shuts down the system (The maximum dc-link voltage allowed by the hardware is 420 V). Setting again the damping ratio to $\zeta = \frac{1}{\sqrt{2}}$ and taking the slow dynamic operational requirements from the fuel cell system into account the bandwidth of the voltage controller can be chosen very low around $f_{b,dc}$ =2-5Hz. Setting the settling time to 2500 samples (one quarter of a second)yields the desired pole placement of the voltage control loop:

$$s_{1,2} = \frac{\omega_n}{\sqrt{2}}(-1 \pm j) \approx 17.77(-1 \pm j) \tag{5.47}$$

$$z_{1,2} = \exp(T_s s_{1,2}) \approx 0.9982 \pm j0.0018 \tag{5.48}$$

Fig. 5.14 shows a diagram of how the dc-link interconnects the DC-DC converter and the inverter (DC-AC).

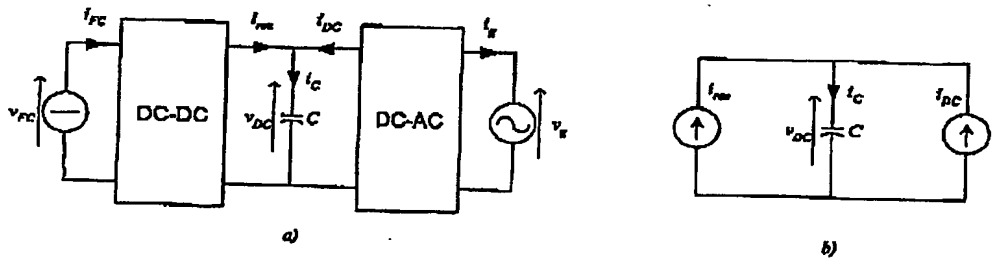


Figure 5.14: *Equivalent circuit for dc-link control.*

The dynamics of the current loop will be neglected during design of the voltage controller since the current loop bandwidth is app. 250 times higher than the outer voltage loop bandwidth. In addition the Push-Pull current control bandwidth is also much higher than the voltage controller bandwidth. Therefore, the equivalent diagram on fig. 5.14.b is used

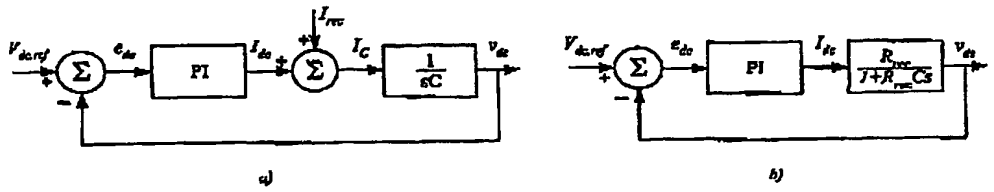


Figure 5.15: *Equivalent circuit for dc-link control.*

as model for the voltage controller.
For perfect resistor emulation and with sinusoidal grid voltage the power balance gives

$$\langle i_{dc} \rangle_{T_g/2} = \frac{\hat{i}_g \cdot \hat{v}_g}{2\langle v_{dc} \rangle_{T_g/2}} \tag{5.49}$$

Thus in steady state there is a simple relation between i_{DC} and i_g. A PI controller is selected in order to achieve a dc voltage error at zero and to have a more smooth dc current reference less sensitive to noise. Fig 5.15.a shows the block diagram of the the dc-link control of the circuit in fig 5.14.b where the rectified current is treated as an disturbance since this parameter is not measured. Othewise it would be obvious to make a feedforward compensation of the rectified current. Making a linear approximation around an operating point of rectified current gives the block diagram in fig. 5.15.b where the resistance $R_{rec} = \frac{v_{DC}}{i_{rec}}$. Also the fictitious resistance R_{rec} can be calculated as

$$R_{rec} = \frac{V_{DC}^2}{P_{rec}} = \frac{V_{DC}^2}{P_{FC}\eta_{DCDC}} \tag{5.50}$$

At full load the fuel cell power is 1 kW and the dcdc converter efficiency is around 96.5% and the dc voltage is 375 V which gives the minimum resistance $\min(R_{rec}) = 146\ \Omega$.
The transfer system transfer function for the voltage control loop then becomes:

$$H_{DC}(s) \triangleq \frac{V_{DC}(s)}{I_{DC}(s)} = R_{rec} \| \frac{1}{sC} = \frac{R_{rec}}{1 + R_{rec}Cs} \tag{5.51}$$

$$H_{DC}(z) = \frac{z-1}{z} \mathcal{Z}\left(\frac{H_{DC}(s)}{s}\right) = R_{rec}\frac{1 - \exp(-\frac{T_s}{R_{rec}C})}{z - \exp(-\frac{T_s}{R_{rec}C})} \tag{5.52}$$

$$= \frac{R_{rec}(1-\beta)}{z-\beta} \tag{5.53}$$

where $\beta \triangleq \exp(-\frac{T_s}{R_{rec}C})$. Again the PI controller can be written as

$$D(z) = K_p \frac{z\left(1 + \frac{T_s}{T_i}\right) - 1}{z - 1} \tag{5.54}$$

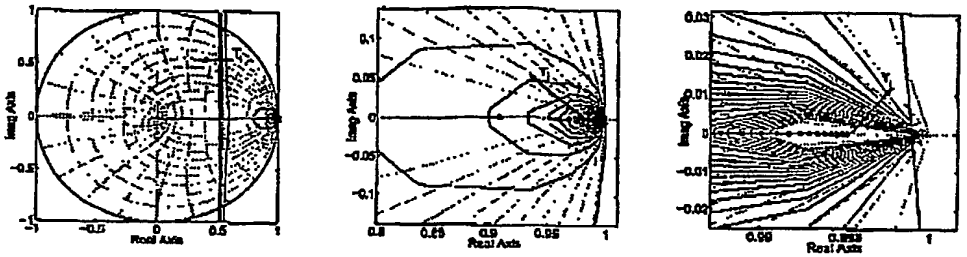


Figure 5.16: *Root locus of voltage loop including delay. a) Different integration times, b) a zoomed view and c) a zoomed view near the desired pole placements.*

Poles	Zeros	K_p	T_i/T_s
0.0025	0.9975	0.0166	400
$0.9982 \pm j0.0018$			

Table 5.4: *System poles and zeros of the voltage control loop*

The open loop transfer function including delay:

$$GH_{+d} = K_p R_{rcc}(1-\beta)\cdot\frac{z\left(1+\frac{T_s}{T_i}\right)-1}{(z-1)(z-\beta)z} = K_p R_{rcc}(1-\beta)\cdot\frac{z\left(1+\frac{T_s}{T_i}\right)-1}{z^3-(1+\beta)z^2+\beta z} \qquad (5.55)$$

Fig. 5.16 show the influence in the root locus by varying the integration time.
The root locus passes the desired pole location when $T_i = 400 \cdot T_s$ which is shows in fig. 5.17.

At a proportional gain at $K_p = 0.0166$ the poles and zeros of the closed loop are listed in tab. 5.4.

Fig. 5.18.a shows step the response of the current control system (red) and the desired step response (blue). The dynamics are a bit different to the specified performance due the the extra pole added from the unit delay. Again, the real pole and the real zero can be compensated in order to make the dynamics match the specifications.
Fig. 5.18.b shows the step response with and without compensation.

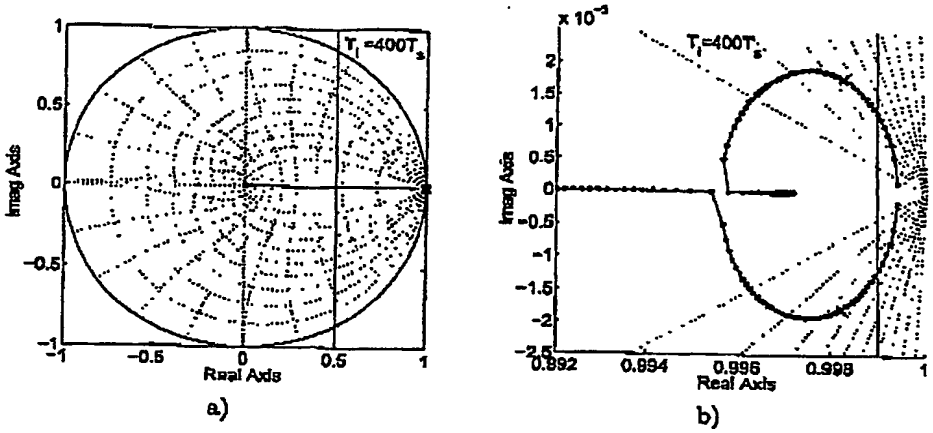


Figure 5.17: *a) Root locus of voltage loop including delay and with a integration time $T_i = 400T_s$. b) a zoomed view near the desired pole placements.*

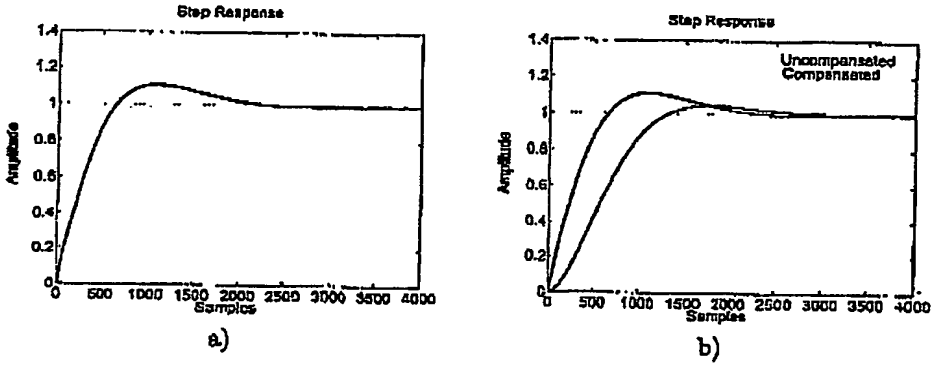


Figure 5.18: *a) Step response of designed voltage loop and b) including compensation.*

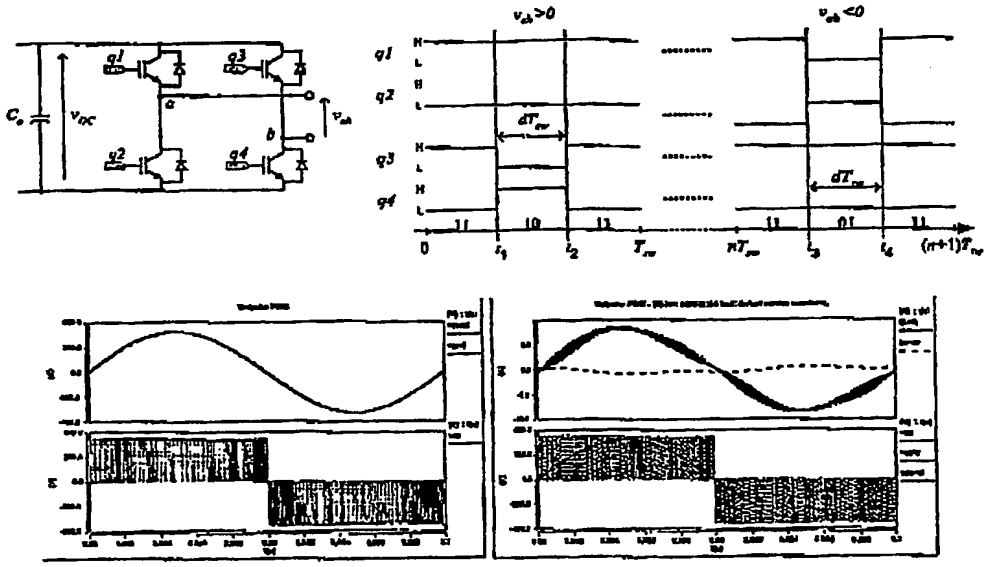


Figure 5.19: *PWM with unipolar voltage switching. Deadtime is excluded from the figure.*

5.7 Inverter Modulation

Shown in fig. 5.19 the inverter realises the voltage v_i by modulating the switches. Here unipolar modulation is used in order to minimize the number of switching instances per switch cycle. Only one branch is switched for each half cycle of the grid period. The gate signals and the corresponding vectors[1] are listed. The vector sequences are

$$11 \rightarrow 10 \rightarrow 11 \qquad \text{for } v_{ab} > 0 \tag{5.56}$$

$$11 \rightarrow 01 \rightarrow 11 \qquad \text{for } v_{ab} < 0 \tag{5.57}$$

The code implemented in Saber to simulate the unipolar modulation is shown in fig. 5.20. Deadtime compensation is eluded in fig. 5.20.

[1]The term vector should not be thought of as a space vector. It is merely a convenient designation for the inverter switch states.

```
if (vabsref>0){
d1=1
d2=0
d3=0
if (vdc>1) d4=vabsref/Vdc
if (d4<0)  d4=0
if (d4>1)  d4=1
schedule_event(time,q2,14_0)
schedule_event(time,q4,14_0)

schedule_event(time,q1,14_1)
schedule_event(time,q3,14_1)

schedule_event(time+0.5*Tsw*(1-d4)-deadtime,q3,14_0)
schedule_event(time+0.5*Tsw*(1+d4)+deadtime,q3,14_1)

schedule_event(time+0.5*Tsw*(1-d4),q4,14_1)
schedule_event(time+0.5*Tsw*(1+d4),q4,14_0)
}
```

```
else{
d1=0
if (vdc>1) d2=abs(vabsref/Vdc)
if (d2<0)  d2=0
if (d2>1)  d2=1
d3=1
d4=0
schedule_event(time,q2,14_0)
schedule_event(time,q4,14_0)

schedule_event(time,q3,14_1)
schedule_event(time,q1,14_1)

schedule_event(time+0.5*Tsw*(1-d2)-deadtime,q1,14_0)
schedule_event(time+0.5*Tsw*(1+d2)+deadtime,q1,14_1)

schedule_event(time+0.5*Tsw*(1-d2),q2,14_1)
schedule_event(time+0.5*Tsw*(1+d2),q2,14_0)
}
```

Figure 5.20: *SABER code for the unipolar inverter modulation.*

5.8 Simulation analysis/results

This section demonstrates the performance of the designed controllers by simulation. Several cases have been investigated:

- The necessity of including a damping resistor.
- Which of the designed controllers to use.
- Grid current performance with different grid impedances.
- Grid current performance with distorted grid.

Ideally, all combinations of these variables should be tested. Figure 5.21 shows the grid current when a distortion in the grid voltage is introduces. This distortion has a frequency at 4kHz which practically corresponds to the resonance frequency of the LCL filter.

The first line period (0-20ms) is simulated without damping but at time=20ms a damping resistor is added, and at time=40ms the distortion is removed. It is obviously from this simulation how effective the damping is. Without testing with a distortion voltage around 4kHz this possible instability could not be known until it appears in reality. But the increasing conducting resistance of the coils in the LCL filter due to skin effect could be enough to damp the filter. This has not been verified and a damping resistance of 38Ω has been chosen.

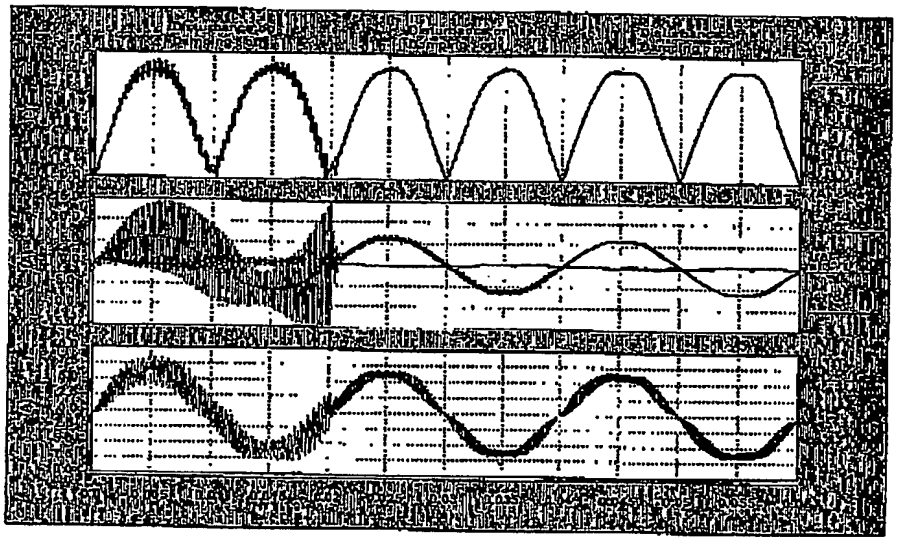


Figure 5.21: *Current loop performance when a noise voltage close to the filter resonance frequency is injected in the grid voltage. The upper plot shows the duty cycle, the middle plot shows the grid current, the reference current and the current error. The lower plot shows the inner inductor current (inverter current). From 0-20ms: The disturbance is active and no damping are used. From 20ms-40ms: damping is added, and from 40ms-60ms: the disturbance is removed.*

5.8.1 Grid current performance

First, performance of the three current controllers in fig. 5.13 is shown with and without compensation. Fig. 5.22 shows the grid current performance without compensation. The simulations are performed at 1000W and each plot shows the reference current, the grid current and the error current.

Fig. 5.23 shows the same simulations as in fig. 5.22 but here is compensation used. In addition, the current reference signal before and after the compensation is shown.

The current controller parameters $T_i = 8T_s$ and $K_p = 14$ seems to provides the best results. Thus, the best grid current performance is achieved with the same controller parameters as found by the simple LR model. The major difference between non-compensated and compensated simulations are a little phase shift on the grid current in the case without compensation.
Based upon these simulation results it is chosen to use $T_i = 8T_s$ and $K_p = 14$ as PI current controller parameters.
Fig. 5.24 shows the performance of the current controller a different power levels. It can be seen that the performance is adequate in that power range.

5.8.2 DC voltage controller performance

Fig. 5.25 shows simulated performance of the dc voltage controller. The upper plot shows the grid current and the output of the dc link controller (amplitude command I_{dc}), the middle plot shows the dc-voltage error and the lower plot shows the reference dc voltage, the dc voltage and partly the absolute value of the grid voltage. A step up in the input current (rectified current) is added at time 0.4 s and the dc voltage is almost settled after 250ms which corresponds to 2500 samples. A step down in the rectified current is added at time 0.75. The æstep upæ shows that the dc voltage does not exceed the maximum limit and the æstep downæ shows that the dc voltage does not fall below the peak of the grid voltage and thereby risking to shut down the system, shortly.

5.9 Conclusion

This chapter have described the control of the grid connected inverter. Special attention have been placed on the current control of the LCL filter. Two controllers have been designed and tested via simulations. The current controller have been tested with and with out background distortion of the grid voltage. In addition, the current controller has also been tested with different line impedanzes and it seems to be operating proporly in every situation. The dc voltage controller has also been tested successfully via simulations. Both controllers are conventional PI controllers.

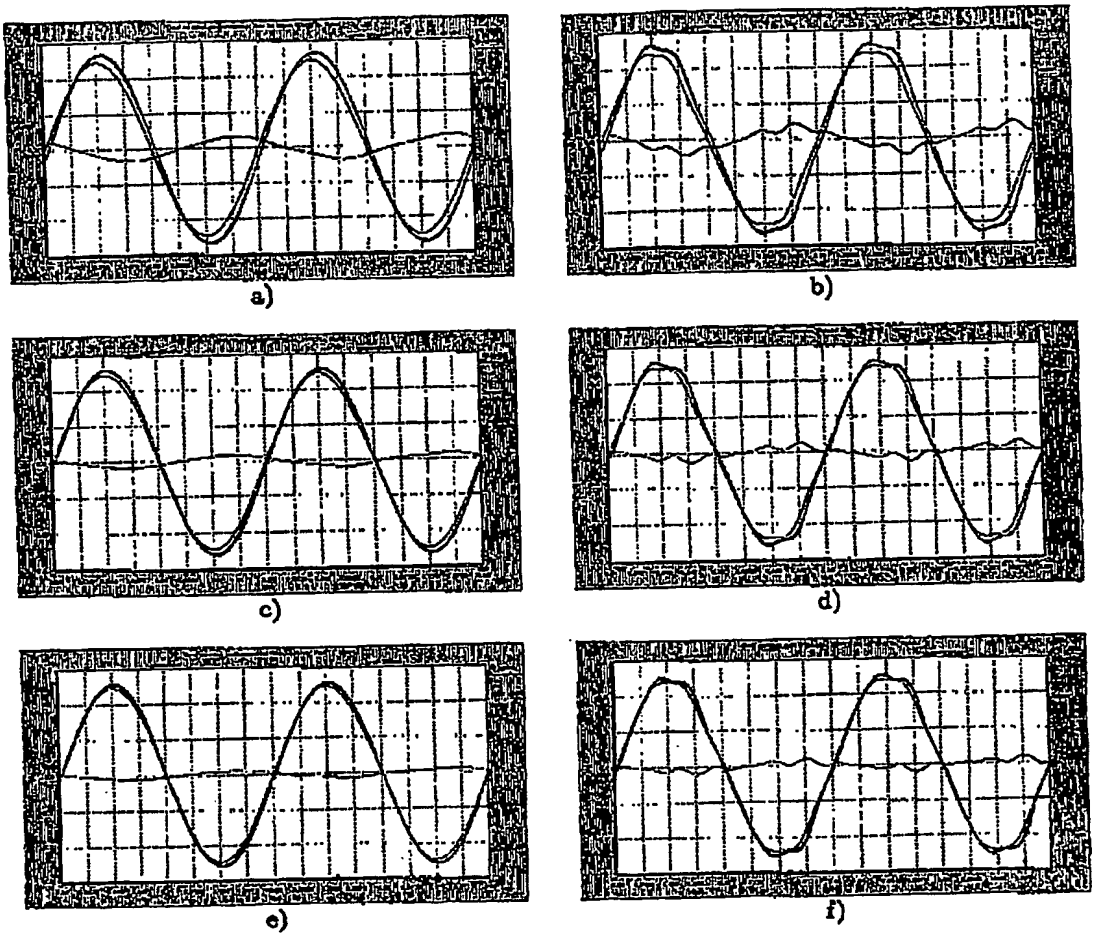


Figure 5.22: *Grid and inverter current with constant current amplitude reference without compensation. The power level 1kW. Simulations a),c) and e) are with ideal grid voltage and simulations b),d) and f) are with distorted grid voltage.*

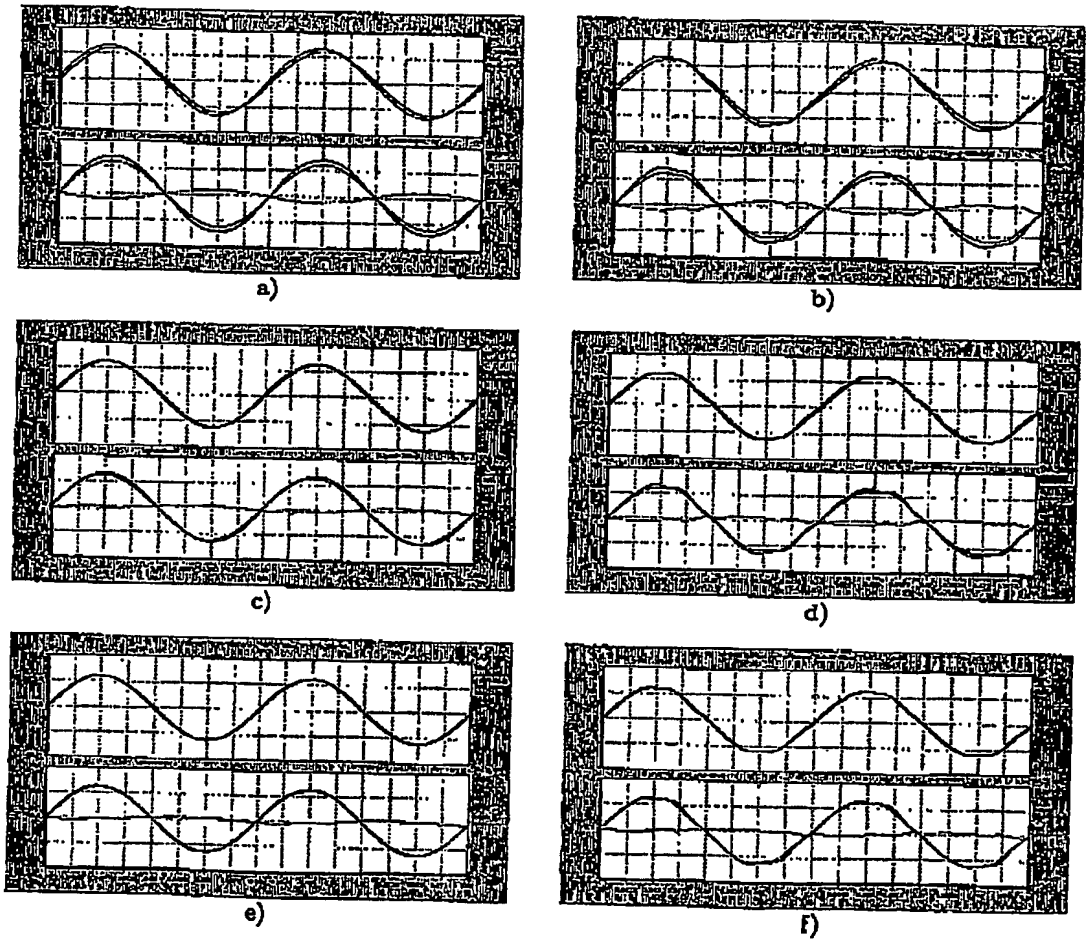


Figure 5.23: *Grid and inverter current with constant current amplitude reference with compensation. The power level 1kW. Simulations a),c) and e) are with Ideal grid voltage and simulations b),d) and f) are with distorted grid voltage.*

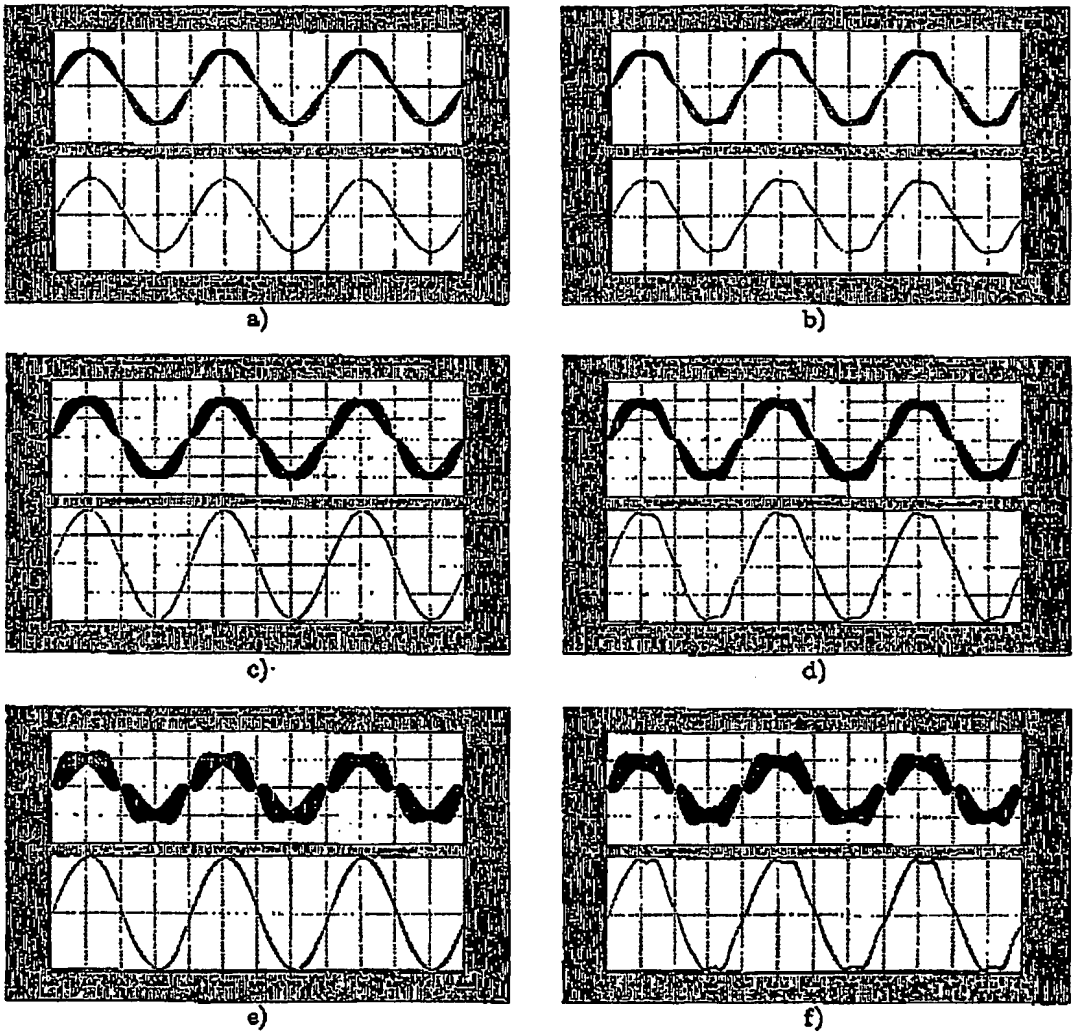


Figure 5.24: *Grid and inverter current with constant current amplitude reference without compensation: a) & b) are for 1000W, c) & d) for 600W and e) & f) for 300W. Simulations a),c) and e) are with ideal sinuoidal grid voltage, and simulations b),d) and f) are with distorted grid voltage (see. fig. 5.1.a). All plots includes three line periods and the grid impedance is changed for each line period.*

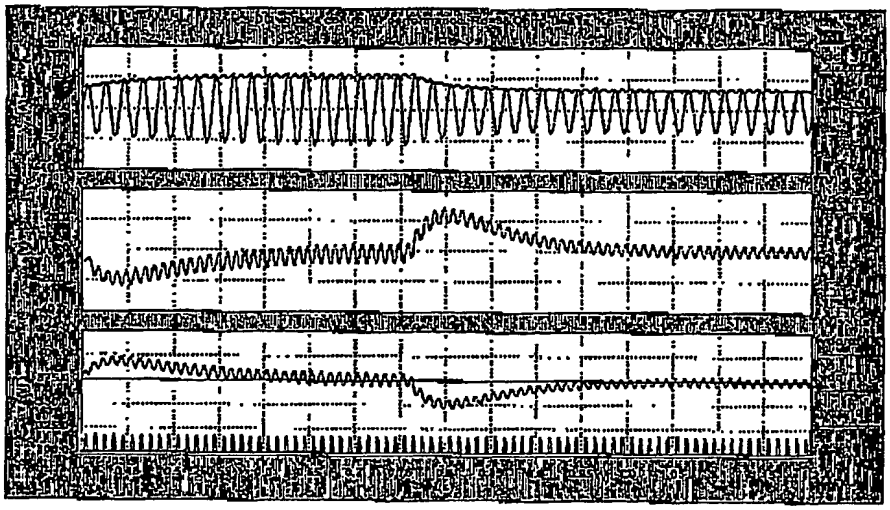


Figure 5.25: *DC-lik control.*

Chapter 7

Evaluation of the first GPI prototype - and next generation

THIS CHAPTER evaluates the performance of the first Green Power Inverter and this prototype will be referred to as the open-prototype due to the open construction.

7.1 Converter Efficiency

Tab. 7.1 shows the overall performance of the open prototype over the whole power range. It should be noted that the VLT fan was running at the three highest power levels.

Power [W]			Efficiency [%]			Grid performance	
P_{FC}	P_{dc}	P_{grid}	η_{DCDC}	η_{inv}	η_{GPI}	THD_i [%]	PF [%]
101.9	96.2	74.6	94.4	77.6	73.2	36.6	90.6
198.4	191.1	166.5	96.3	87.0	83.9	18.5	97.5
303.7	293.0	268.5	96.5	91.3	88.4	10.3	99.1
400.9	388.3	360.0	96.8	92.7	89.8	7.8	99.5
502.6	485.1	455.1	96.5	93.8	90.6	7.0	99.7
601.7	580.5	545.9	96.5	94.0	90.7	6.7	99.8
702.3	675.6	637.1	96.2	94.3	90.7	6.6	99.8
804.8	766.7	726.6†	95.3	94.8	90.3	4.0	99.8
902.1	850.7	802.9†	94.3	94.4	89.0	3.9	99.9
1001.0	923.8	870.4†	92.3	94.2	87.0	3.8	99.9

Table 7.1: *Measured overall GPI performance. Background distortion of the grid voltage is around THD_v =3%. † VLT fan was running.*

In tab. 7.1 P_{FC} is the power entering the DC-DC converter, P_{dc} is the power out from

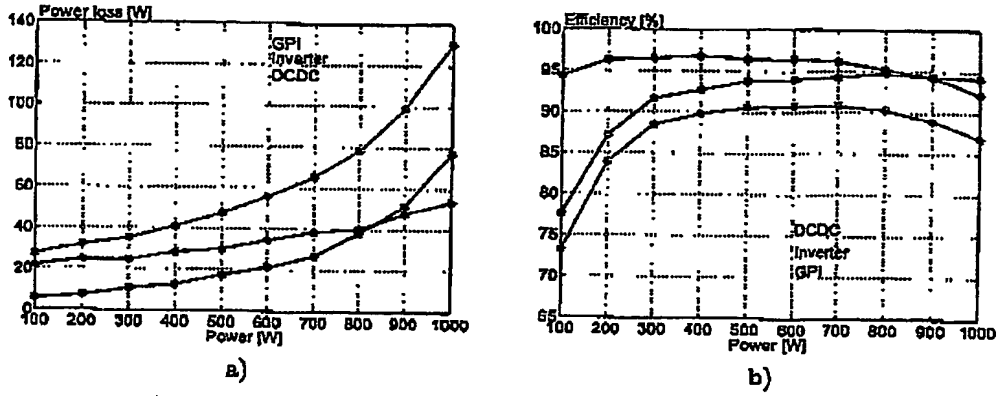


Figure 7.1: *Measured overall GPI performance including VLT power supply. a) Power losses in the system and b) efficiency.*

the DC-DC converter and P_{grid} is the power delivered to the grid. The efficiency of the DC-DC converter η_{DCDC}, the efficiency of the VLT η_{inv} are listed along with the overall GPI efficiency η_{GPI}. Power loss and efficiency from tab. 7.1 are visualized in fig. 7.1.
It should be noted that the inverter efficiency listed in this chapter includes internal VLT supply and fan power. Fig. 7.2 illustrates the laboratory system.

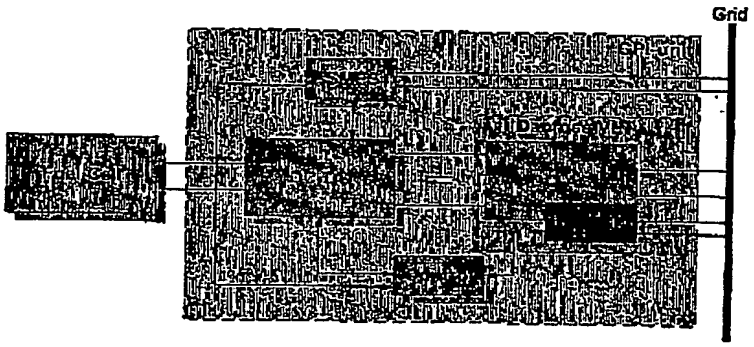


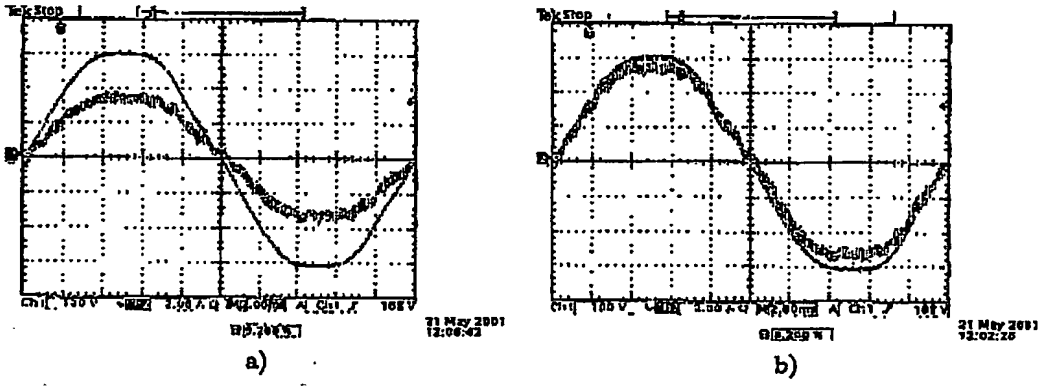
Figure 7.2: *Schematic of the implemented laboratory system.*

As can be observed from this figure, the VLT includes an internal power supply which is not intended to be a part of the system. This power supply decreases the measured efficiency. Since this power supply will not be included in a final GPI the inverter. Thus,

the inverter and the GPI efficiency in tab. 7.1 and in fig. 7.1 are not realistic numbers and these numbers should be corrected in order to give a realistic value (this will be illustrated later). From tab. 7.1 and fig. 7.1 it is obvious that the GPI efficiency peaks at the desired power level at 600 W.

7.2 Grid Performance

Fig. 7.3 shows the grid current and grid voltage at 600W and 1000W respectively. This figure illustrates the resistor emulation as the grid current and voltage is in phase and the waveshapes are alike. The are some high frequency oscillations in the grid current at the switching frequency. This oscillation are due to noise in the feedback in the prototype. Especially the feedforward of the grid voltage (cf. fig. 5.8 on page 85) is relative sensitive to noise. This can and must be improved in the next generation.



a) b)

Figure 7.3: *Grid current at a) 600W and b) 1000W.*

Fig. 7.4 shows the grid performance of the GPI in terms of power factor and current THD (the numbers are from tab. 7.1).

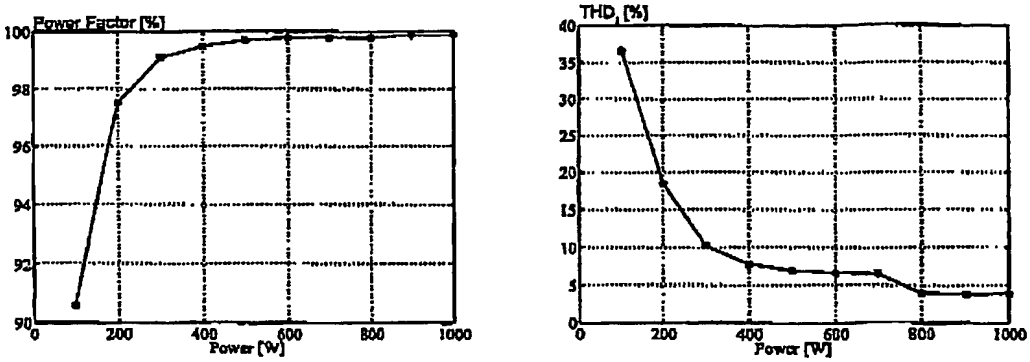


Figure 7.4: *Power factor and THD_I*

7.3 Fuel Cell Voltage Control

The previous results have treated steady state operation in terms of fuel cell voltage and current. The GPI must follow a voltage reference set by the fuel cell control system by adjusting the fuel cell current. Fig. 7.5 shows a step in the fuel cell voltage reference. The figure shows the input and the output of the GPI: the fuel cell voltage and the grid current. The fuel cell voltage is ramped slowly and the ramping time changeable by software. The ramping time in the present prototype is set to around 30 seconds from the lowest power level to peak power.

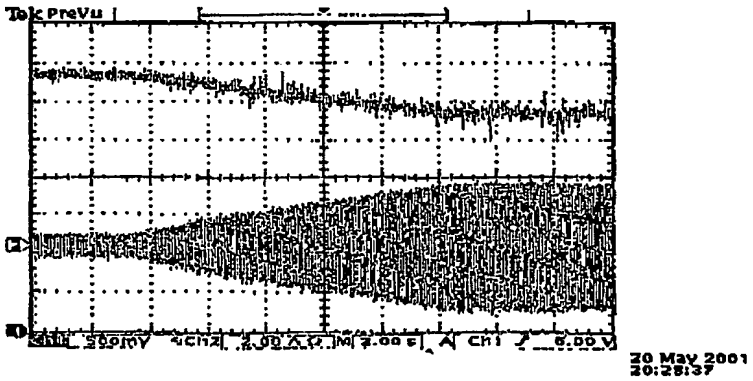
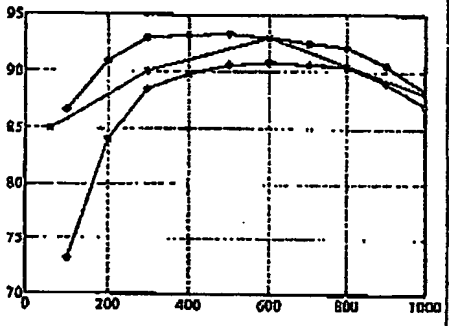


Figure 7.5: *Fuel cell voltage control. Yellow: fuel cell voltage, green: grid current.*



a)

Power [W]	Efficiency [%] Measured	Estimated	Demands
100	73.2	86.9	Ø
200	84.0	91.1	Ø
300	88.4	93.0	90.0
400	89.8	93.3	Ø
500	90.5	93.3	Ø
600	90.8	93.1	93.0
700	90.6	92.6	Ø
800	90.4	92.1	Ø
900	89.0	90.6	Ø
1000	87.0	88.4	88.0

b)

Figure 7.6: *Efficiency evaluation and estimation for next generation. a) Blue:measured, red:compensation for power consumption in VLT and green: demands.*

7.4 Improvements for next generation

Fig. 7.6.a shows the measured efficiency, the requirements and the estimated efficiency by compensation of the VLT power supply: The VLT power consumption has been measured and replaced by the measured power consumption of the designed SMPS (cf. chapter 2). As can be observed, the efficiency will fulfill the requirements by replacing the VLT by an integrated inverter.

7.5 Conclusion

The performance of the first open-prototype has been verified by measurements. The efficiency is high in a wide input power range but due to an additional power supply in the VLT the measured efficiency is not realistic numbers. Adjusting for the power consumption from the VLT power supply alone makes the GPI meet the specifications for efficiency. The grid performance is high in the whole power range with a near unity power factor. Dynamic operation have also been verified by a step in the fuel cell voltage.Thus, the expected GPI fulfill the requirements regarding efficiency and grid performance.

923	TBR	20-maj		
924	TTH	20-maj		
925	VBB	20-maj		
926	ANE	20-maj		
927	HNJ	27-maj		
928	ISL	27-maj		
929	JAL	27-maj		
930	KRS	27-maj		
931	LIJ	03-jun		
932	LOS	03-jun		
933	LVJ	03-jun		
934	RSN	03-jun		
935	SJ	11-jun		
936	TBR	11-jun		
937	TTH	11-jun		
938	VBB	17-jun		
939	ANE	17-jun		
940	HNJ	17-jun		
941	ISL	24-jun		
942	KRS	24-jun		
943	LFH	24-jun		
944	LIJ	01-jul		
945	LOS	01-jul		
946	LVJ	01-jul		
947	RSN	15-jul		
948	SJ	15-jul		
949	TBR	15-jul		
950	TTH	22-jul		
951	VBB	22-jul		
952	ANE	22-jul		
953	HNJ	29-jul		
954	ISL	29-jul		
955	KRS	29-jul		
956	LIJ	05-aug		
957	LOS	05-aug		
958	LVJ	05-aug		
959	RSN	12-aug		
960	SJ	12-aug		
961	TBR	12-aug		
962	TTH	19-aug		
963	VBB	19-aug		
964	ANE	19-aug		
965	HNJ	26-aug		
966	ISL	26-aug		
967	KRS	26-aug		
968	LFH	02-sep		
969	LIJ	02-sep		
970	LOS	02-sep		
971	LVJ	09-sep		
972	RSN	09-sep		
973	SJ	09-sep		
974	TBR	16-sep		
975	TTH	16-sep		
976	VBB	16-sep		
977	ANE	23-sep		
978	HNJ	23-sep		

979	ISL	23-sep
980	KRS	30-sep
981	LIJ	30-sep
982	LOS	30-sep
983	LVJ	
984	RSN	
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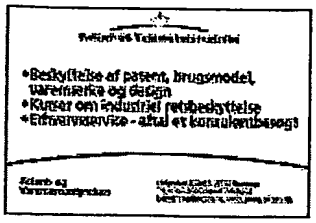
Info

Info : **Patent- og Varemærkestyrelsen**
Adresse: Helgeshøj Allé 81
2630 Taastrup
Telefon: (+45) 4350 8000
Mobil:
Fax: (+45) 4350 8001
Web-site: www.dkpto.dk
E-mail: pvs@dkpto.dk
CVR nr.: 17039415



Beskyttelse af: Patent, brugsmodel, design, varemærke. Kurser om industriel eneretsbeskyttelse. Erhvervsservice - aftal konsulentbesøg

Profil

Oplysninger

Antal ansatte: 280
Etablerings år:
Registrerings år:
Eksportandel:
Bankforbindelse:
Girooplysninger: 8989923
CVRnr.: 17039415
P nr.: 1003407818
Flere telefonnr.:
Flere faxnr.:
Flere e-mail adr.:
Flere web adr.:

Personer

Topledelse: Direktør Mogens Kring
Henrik Dahl Sørensen
Niels Ravn
Marketing: Lone Hartung
Salg: Lone Hartung
Indkøb: Steen Halk Pedersen
Ansvarlig ledelse - Off.: Direktør Mogens Kring

Supplerende oplysninger:

Patent- og Varemærkestyrelsen
Helgeshøj Allé 81, 2630 Taastrup
Tlf. 43 50 80 00 (Telefontid: man-fre 9-16)
Fax: 43 50 80 01
E-mail: pvs@dkpto.dk
WEB: www.dkpto.dk
Læsesal man-fre 9-14, tor 9-16
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